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CSE7761

User Manual

Wide voltage, high performance energy metering chip REV 2.0

芯海科技（深圳）股份有限公司
地　址：深圳市南山区蛇口南海大道1079号花园城数码大厦A座9楼
电　话：+(86 755)86169257　　传　真：+(86 755)86169057
网　站：www.chipsea.com　　邮　编：518067
微信号：芯海科技

Revision History

History	Modifications:	Version Date
REV 1.0	Initial version:	2018-04-01
REV 2.0	Verify and calibrate performance	2019-06-13
REV2.1	indicators. Correct zero-crossing detection delay relative to actual signal.	2019-07-08

Table of contents

1 Product Overview

1.1 Features Overview

ÿ Clock Management

Built-in crystal oscillator and external crystal oscillator functions are optional.

ÿ Metering function

- Provides two channels of active energy: active energy error is within 5000:1 dynamic range error <0.1%

- Provides two channels of active power: Channel A active power and Channel B active power, Channel B is closed by default - Provides apparent power, power factor, phase angle, and selects the channel to be calculated through commands: Channel A or Channel B - Provides waveform data of one channel of voltage and two channels of current - Provides instantaneous values of one channel of voltage and two channels of current effective value - Provides instantaneous values of two channels of active power and one channel of apparent power

The instantaneous value of apparent power is calculated by selecting the channel: Channel A or Channel B.

- Provides measurement of one voltage and two current RMS values: RMS error <0.1% within a 1000:1 dynamic range - Provides active power overload signal indication, and selects the calculation channel through commands: channel A or channel B - Provides zero-crossing detection signal, line frequency, overvoltage indication, and undervoltage indication for the voltage channel - Provides zero-crossing detection signal and overcurrent indication for two current channels

ÿ Communication interface

- SPI interface, the fastest supported frequency is 890KHz - UART interface, baud rate is 4800Hz, 9600Hz, 19200Hz, 38400Hz.

ÿ With system correction function and phase compensation function; startup and creeping current are adjustable

ÿ Support software reset ÿ 1 high-precision comparator ÿ Built-in temperature sensor ÿ PGA of voltage and two current channels optional: 1, 2, 4, 8, 16 ÿ Multiple interrupts: voltage zero-crossing interrupt, overvoltage interrupt, undervoltage interrupt, current zero-crossing interrupt, overcurrent interrupt, active power overload Interrupt, instantaneous data update interrupt, voltage/current effective value and power average value update interrupt

ÿ Built-in 1.25 reference voltage ÿ Working voltage: VDD=5V/3.3V ÿ Package: SSOP16

1.2 Functional Description

CSE7761 is a single-phase multifunctional energy metering chip, which integrates 3-way sigma-delta ADC, power calculator, energy One SPI interface and one UART interface.

The CSE7761 chip can be used to accurately calculate the voltage RMS, current RMS, active power, apparent power, and power factor. It can measure power, provide high-speed voltage and current waveform data and instantaneous data of voltage RMS, current RMS, active power and apparent power, provide two-way active energy measurement, and can also provide power factor, phase angle, voltage overvoltage, current overcurrent, active power

Output of parameters or indication signals such as power overload, voltage undervoltage, voltage line frequency, voltage zero crossing, current zero crossing and peak-to-peak value.

1.3 Functional Block Diagram

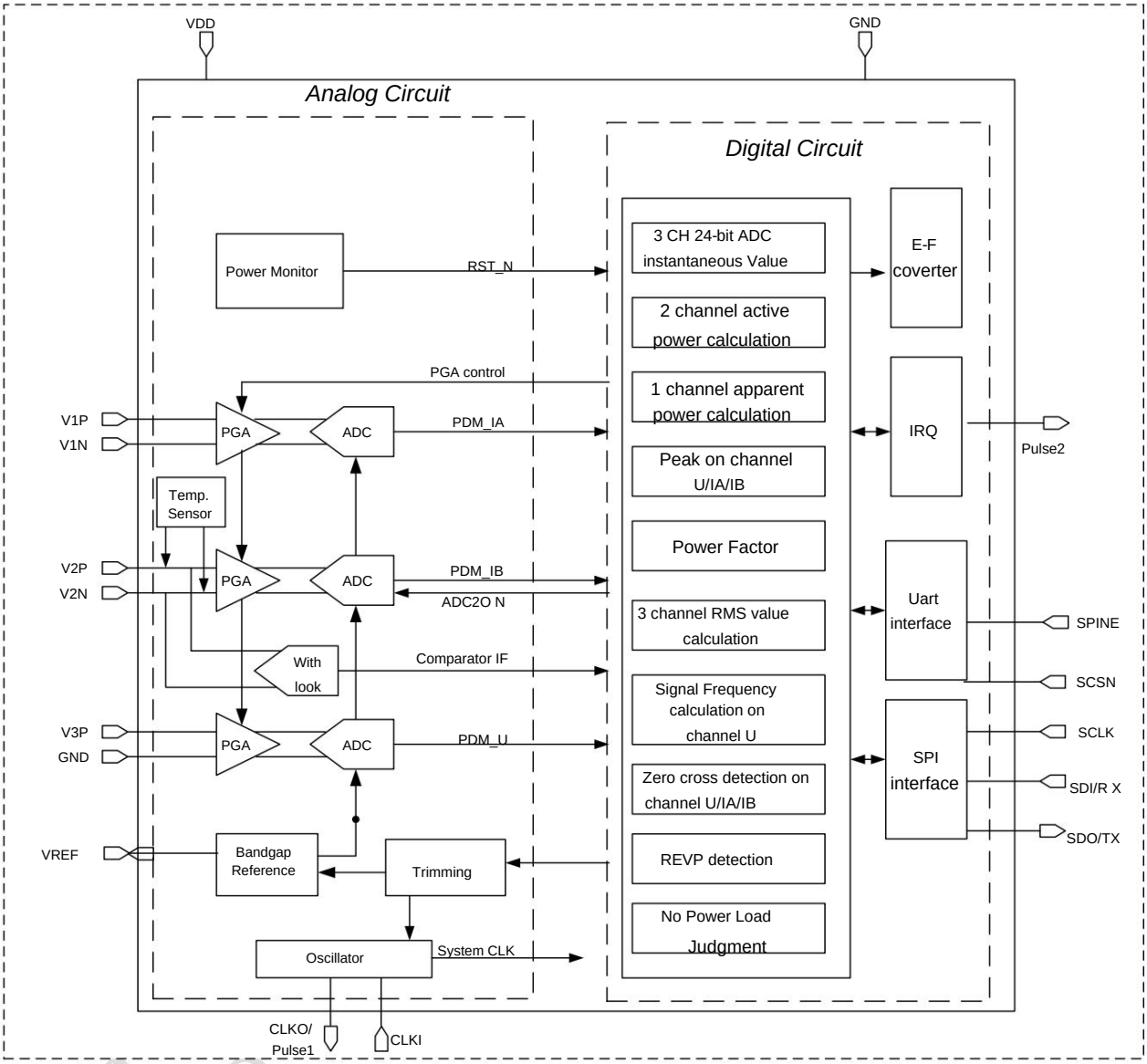


Figure 1-1 Chip block diagram

1.4 Product model, package and **PIN** configuration

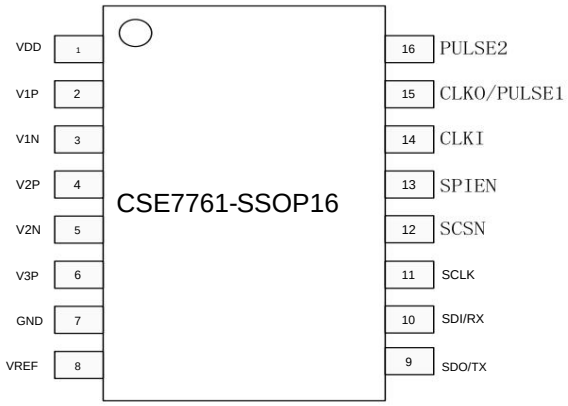


Figure 1-2 CSE7761-SSOP16 package PIN diagram

Table 1-1 CSE7761-SSOP16 Pin Description

Pin Name **I/O**		**SSOP16**	describe
VDD	P	PIN1	Chip power supply, operating voltage range 3V-5.5V, typical voltage 5V or 3.3V, ensuring the power supply ripple is within ±10%.
V1P V1N	I	PIN2 PIN3	Analog input pin of current channel A; fully differential input mode is adopted, normal operation The maximum input Vpp is ±800mV/PGA, and the maximum withstand voltage is ±6V
V2P V2N	I	PIN4 PIN5	The analog input pin of current channel B or the input pin of the comparator detection or the internal Temperature sensor input; fully differential input mode, maximum input for normal operation Input Vpp is ±800mV/PGA, maximum withstand voltage is ±6V
V3P	I	PIN6	Analog input pin of voltage channel; the maximum input Vpp for normal operation is ± 800mV/PGA, maximum withstand voltage is ±6V
GND	P	PIN7 Chip ground	
VREF	P	PIN8	1.25V reference voltage output, this pin should be connected in parallel with a capacitor of at least 1μF 0.1μF capacitor for decoupling.
SDO/TX	THE	PIN9	SPI interface data output or UART data output terminal TX SPINE / SCSN / Description 1 / / SPI Data Output 1 / 0 1 / High impedance output 0 / x / UART data output
SDI/RX	I	PIN10	SPI interface data input or UART data input terminal RX SPINE / SCSN / Description 1 / x / SPI Data Input 0 / x / UART data input

<table>
<tr><td>SCLK</td><td>I</td><td>PIN11</td><td>SPI interface clock input
<table>
<tr><td>SPINE</td><td>SCLK</td><td>SCSN</td><td>describe</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>SCLK: SPI clock input
SCSN:SPI chip select signal</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>The baud rate of UART is 38400</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>The baud rate of UART is 19200</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>The baud rate of UART is 9600</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>The baud rate of UART is 4800</td></tr>
</table></td></tr>
<tr><td>SCSN</td><td colspan="3">I PIN12 SPI interface chip select signal or UART baud rate selection signal</td></tr>
<tr><td>SPINE</td><td colspan="2">I PIN13</td><td>SPI interface enable signal, built-in pull-down resistor
=1, the communication mode of CSE7761 is SPI;
=0, the communication mode of CSE7761 is UART;</td></tr>
<tr><td>CLKI</td><td colspan="2">I PIN14</td><td>External crystal input or digital function output: When CLKI=0, use the internal
When a sine wave is detected on CLKI, the external crystal oscillator function is turned on.
The typical value of crystal frequency is: 3.579545MHz.
The typical value of external capacitance is 22pF, and the internal integrated jumper resistor does not need to be added externally.
Jumper resistor. The ESR of the external crystal is required to be less than 50 ohms.</td></tr>
<tr><td>CLKO/PULSE1 OR PIN15</td><td></td><td></td><td>Output of external crystal or digital function output
<table>
<tr><td>CLKI Description</td><td></td></tr>
<tr><td>0</td><td>Digital function output</td></tr>
<tr><td>Non-0 Output terminal of external crystal oscillator</td><td></td></tr>
</table></td></tr>
<tr><td>PULSE2</td><td colspan="2">It is PIN16</td><td>Digital function output, with 4.2mA (@VDD=5V)/
1.9mA (@VDD=3.3V) source and sink current capability.</td></tr>
</table>

1.5 Typical application diagram

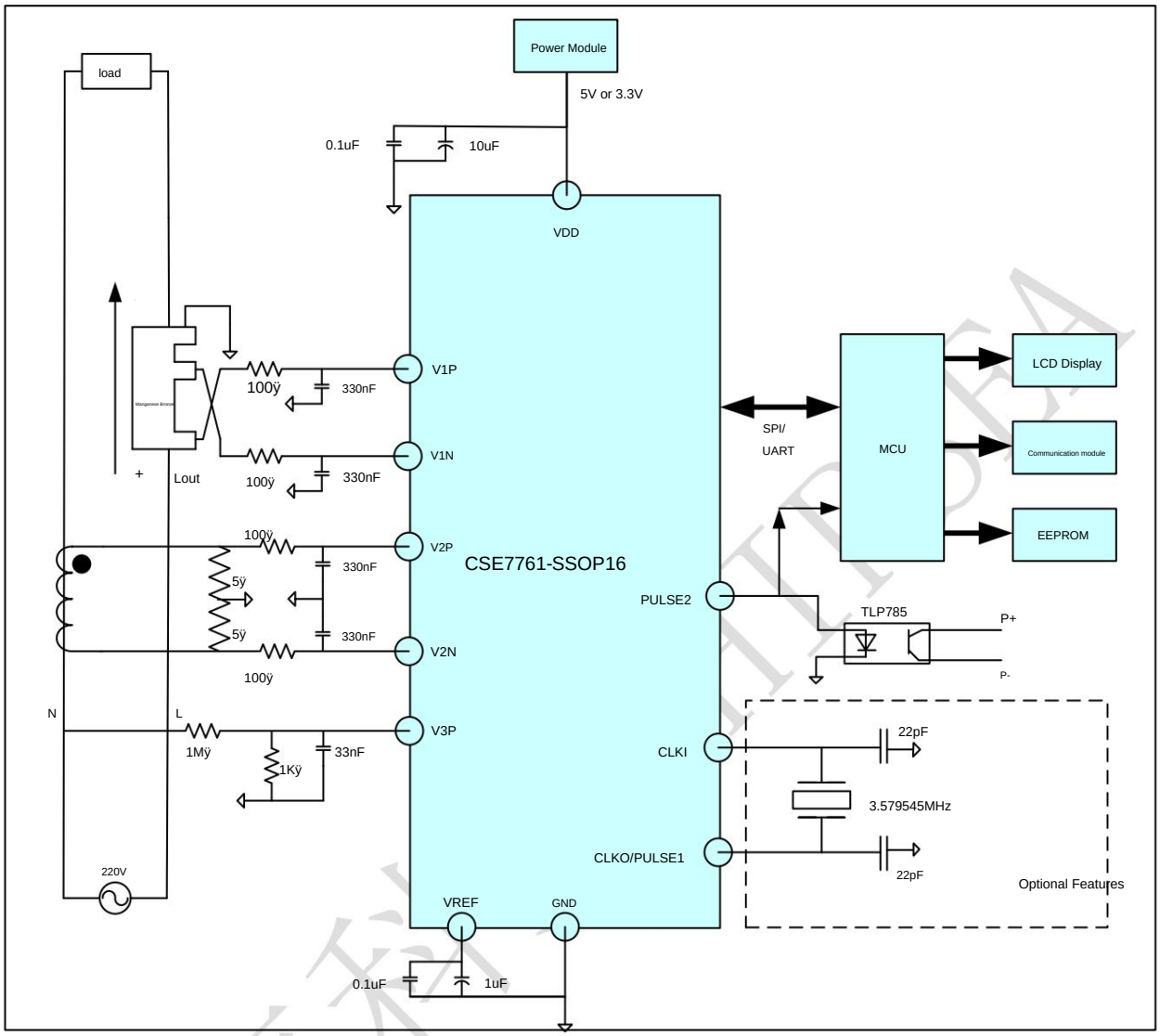


Figure 1-3 Typical CSE7761 anti-electricity theft application diagram

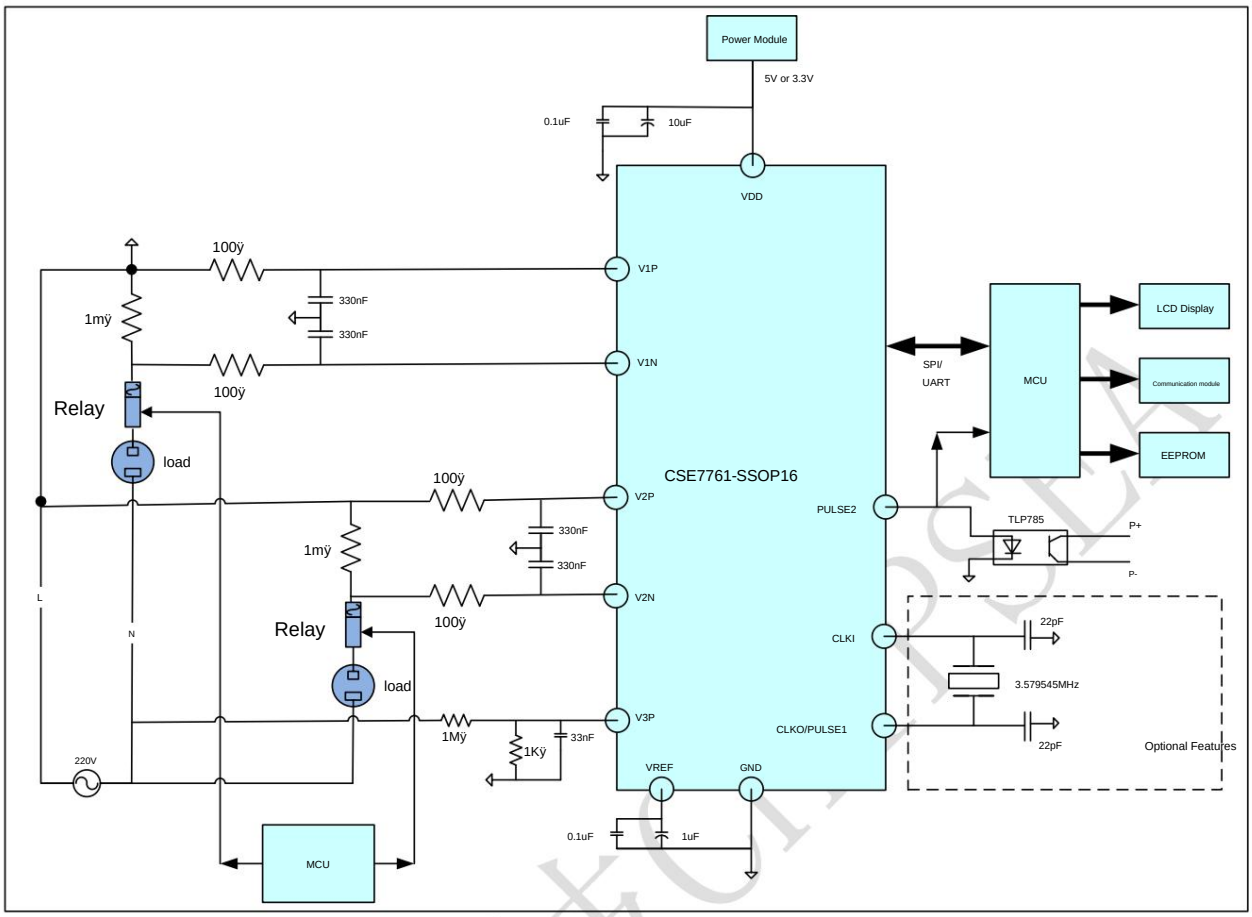


Figure 1-4 Schematic diagram of CSE7761 dual-channel metering typical application

2. Function Overview

2.1 Reset the system

The chip has power-up/power-down reset and instruction global reset modes.

1. The power-on reset threshold voltage of the chip is 2.9V, the power-off reset threshold voltage is 2.7V, and the hysteresis voltage is 0.2V, as shown in the figure below;

2. After the chip receives the reset command, it resets immediately and leaves the reset state after two system clocks.

When any global reset occurs, the registers are restored to the reset initial values and the external pin levels are restored to the initial states.

RST in the system status register is the reset flag: when the power-on reset or instruction reset is completed, this position is 1 and cleared after reading.

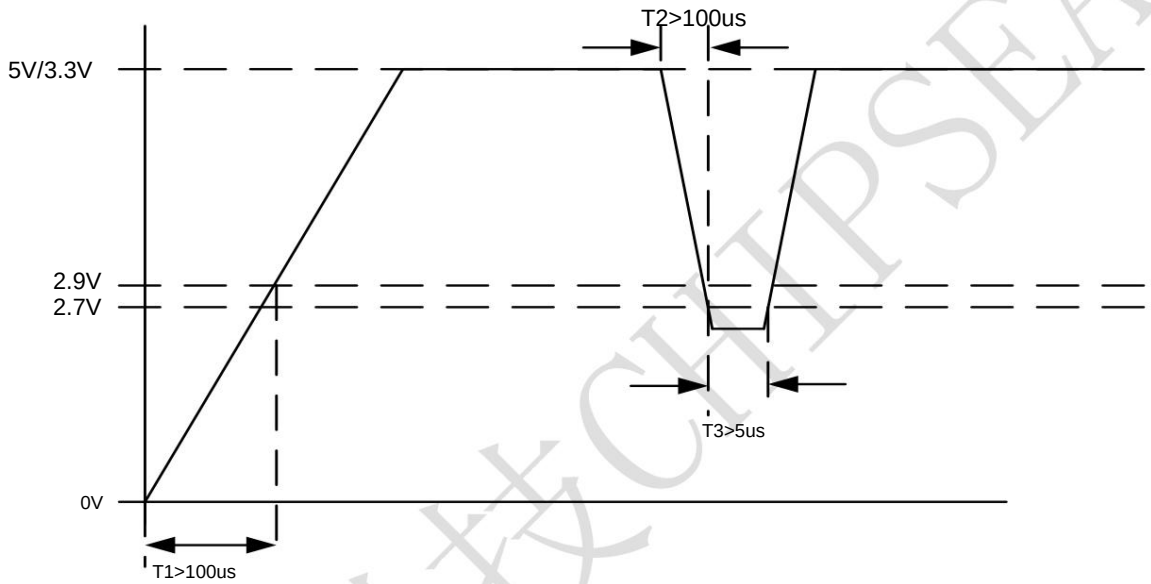


Figure 2-1 Power-on/power-off reset diagram

2.2 Implementation of the clock system

CSE7761 can use an external crystal oscillator: the typical crystal frequency is 3.579545MHz, the maximum external capacitance is no more than 47pF, typical

The value is 22pF, with an internal integrated jumper resistor. No external jumper resistor is required. The ESR of the external crystal is required to be less than 50 ohms.

CSE7761 can also use the built-in crystal oscillator (CLKI=0): the typical frequency is 3.579MHz;

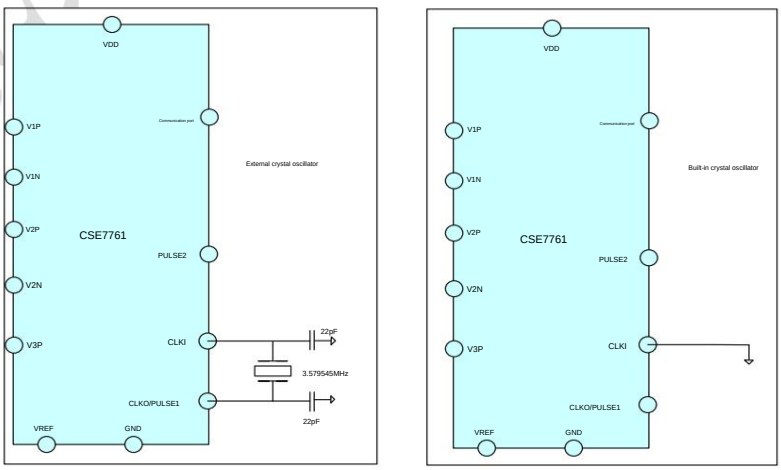


Figure 2-2 Crystal oscillator selection diagram

2.3 Analog-to-Digital Conversion

CSE7761 includes three ADC channels. Current channel A and current channel B are used for current sampling, and voltage channel is used for voltage sampling. The ADC converts the input analog signal into a continuous serial stream of 1s and 0s (PDM), which is then input into the digital circuit for processing to form various Parameters for energy measurement.

The on/off of current channel B is controlled by the ADC2ON register bit in the system control register.

The maximum signal input amplitude of the three ADCs is 800mV peak-to-peak (when PGA=1).

By configuring the bit8~bit6, bit5~bit3, bit2~bit0 in the system control register (SYSCON 0x00H), the three The ADC PGA of each channel is configured, and the gain factor can be selected in 5 levels: 1, 2, 4, 8, 16. The gain factor of current channel A is The default gain magnification of current channel B and voltage channel is 1x.

Table 2-1 Gain PGA Configuration Description

Gain **PGA VREF** Full-scale differential input signal peak-to-peak **PGAIA**				**PGAIB**	**PGAU**
1	1.25V	800	000	000	000
2		400	001	001	001
4		200	010	010	010
8		100	011	011	011
16		50	1xx	1xx	1xx

2.4 channel switching

CSE7761 switches the current channel through special commands to realize phase angle, apparent power, power factor, instantaneous active power, Current channel selection for instantaneous apparent power. The currently selected current channel can be queried through the SYSStatus register bit Channel_sel.

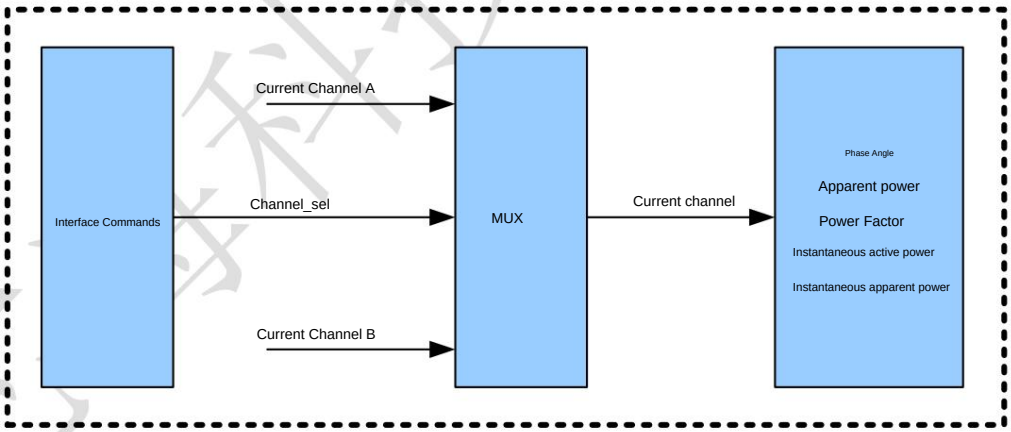


Figure 2-3 Channel switching diagram

2.5 Active power

CSE7761 provides two channels of active power calculation and correction, namely the calculation and correction of active power of current channel A and voltage channel A. Calculation and correction of active power of current channel B and voltage channel.

The registers also include two sets of phase correction, A/B, active offset correction, active gain correction, creeping judgment and average power registers.

In addition, in order to ensure the consistency of the two channels, a gain correction register IBGain for current channel B is also provided.

Note: When ADC2ON=0, the current channel B ADC does not work, and the functions related to the current channel B do not work either.

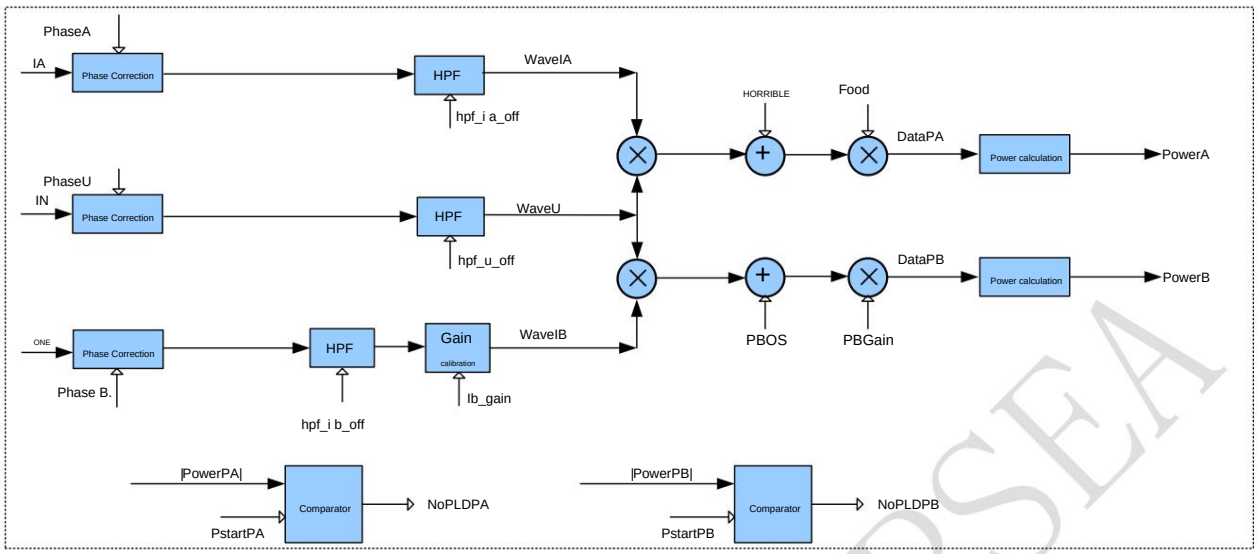


Figure 2-4 Active power calculation block diagram

2.6 Effective value

CSE7761 provides three channels of true RMS parameter output, the corresponding registers are RmsIA, RmsIB and RmsU.

The number of bits is 24 bits, and the update frequency can be selected: 3.4Hz, 6.8Hz, 13.6Hz, 27.2Hz.

CSE7761 also provides two current channels' effective value offset calibration registers, the corresponding registers are RmsIAOS and RmsIBOS.

The register size is 16 bits.

Note: Channel B gain correction (IBGain) will affect the output of RmsIB. Other phase correction, power gain correction, power

Offset correction etc. will not affect the calculation result of the effective value.

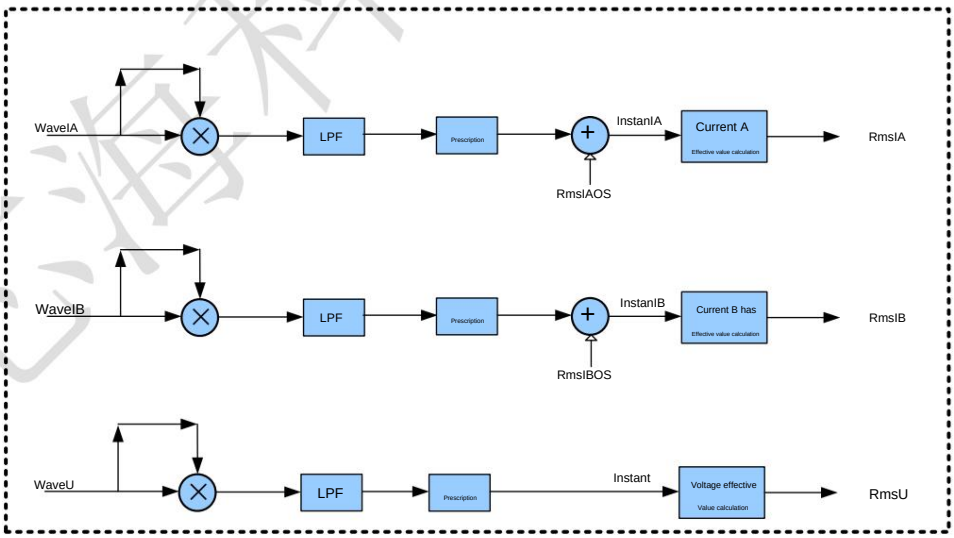


Figure 2-5 Effective value calculation block diagram

2.7 Apparent power and power factor

CSE7761 provides one channel of apparent power and power factor calculation (to calculate the power factor, you must first configure PfactorEN=1):

Select the channel for calculation: channel A or channel B. PowerFactor is a 24-bit signed decimal, with the highest bit being the sign bit. When PF=7FFFFFH, it means the power factor is 1.0; when PF=800000H, it means the power factor is -1.0; when PF=400000H, it means the power factor is 0.5; in the creeping state it is 7FFFFFH;

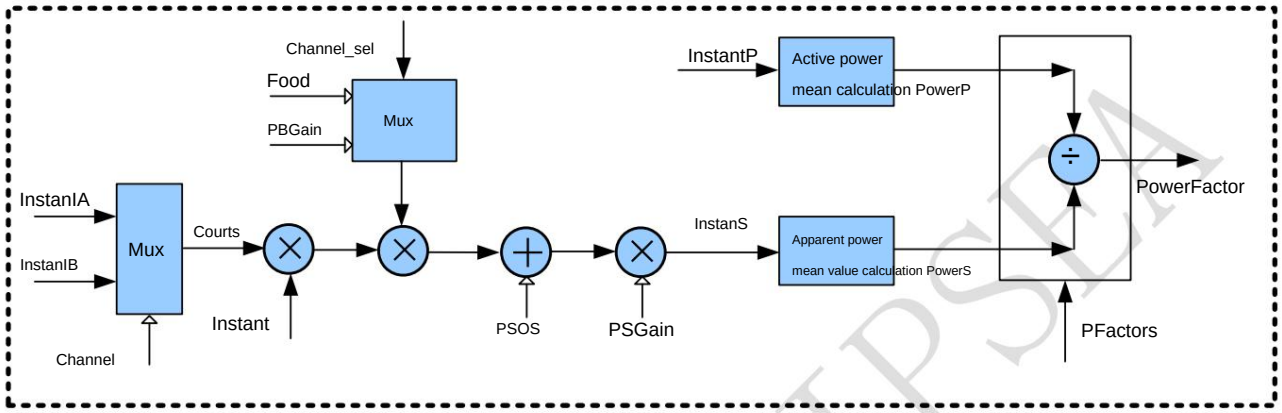


Figure 2-6 Apparent power and power factor calculation diagram

2.8 Energy calculation

The relationship between PFCntPx, HFConst, pulse output, and energy register:

When 2*|PFCntPx| = HFConst, PFx has a pulse output. At the same time, the energy registers EnergyPx and EnergyPx2 are incremented by 1. The relationship between pulse output, energy registers, Prun and Pstart is:

The active energy registers and PFx outputs are also controlled by Prun and Pstart.

When Prun=0 or |PowerPx| is less than PxStart, PFx does not output pulses, and PFCntPx and the active energy register do not increase. Reverse indication: When the active power is negative, the REVPx bit of the EMUStatus register will become 1. The REVPx bit is the same as the PFx pulse.

Step update. PFx output meets error! Reference source not found. Timing relationship:

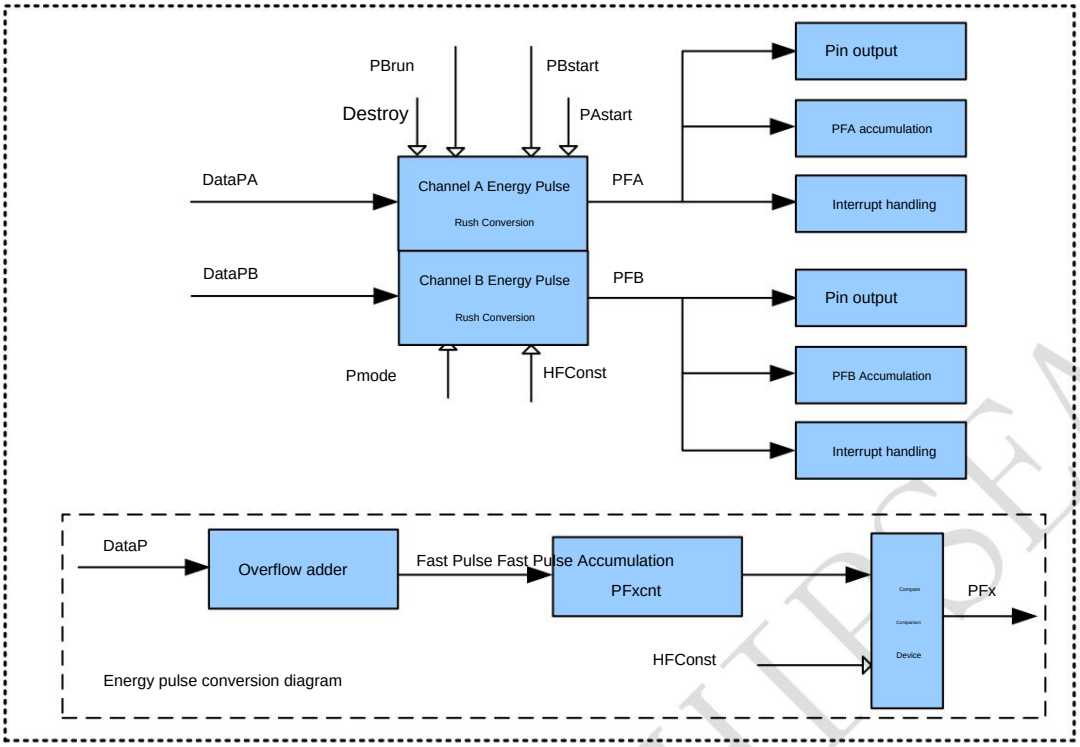


Figure 2-7 Energy calculation block diagram

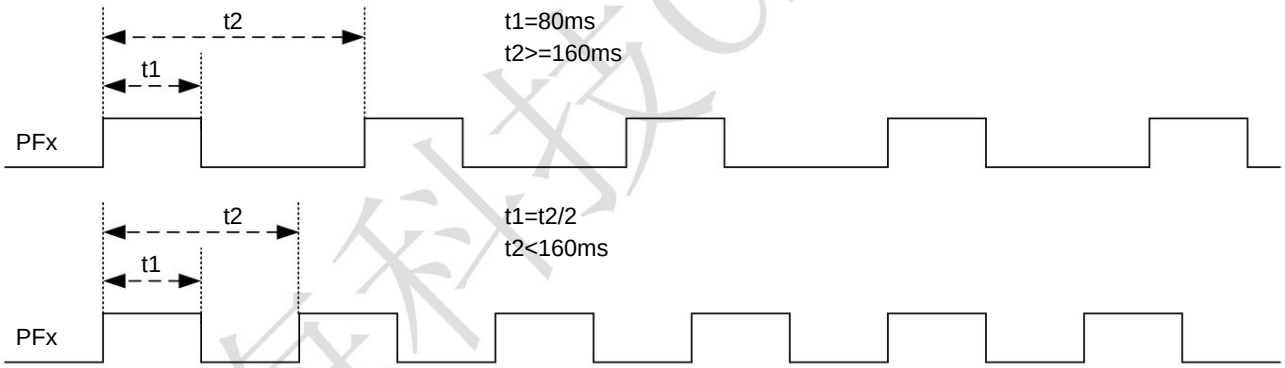


Figure 2-8 PFx output timing diagram

Note: When the pulse output period is less than 160ms, the pulse is output in the form of 50% duty cycle.

2.9 Zero-crossing detection, phase angle, voltage frequency measurement (turn on the instantaneous data function first)

The CSE7761 voltage channel, current channel A, and current channel B all have zero-crossing detection, which can be set by configuring the ZXEN register of EMUCON2.

The zero-crossing detection function can be turned on/off. Four zero-crossing output modes can be selected by configuring the ZXD1 and ZXD0 register bits:

Error! Reference source not found.

CSE7761 can measure the phase angle between voltage channel and current channel A or current channel B (must configure ZXEN=1).

To measure the phase angle, you need to configure ZXEN=1. The register Angle represents the phase angle between the voltage channel and the current channel A or current channel B.

Angle, when the line frequency is 50Hz, the resolution is 0.0805°; when the line frequency is 60Hz, the resolution is 0.0965°.

CSE7761 realizes the measurement of voltage channel frequency (must configure ZXEN=1), measures the fundamental frequency, and the measurement bandwidth is 250Hz.

Read the value of Ufreq to determine the voltage frequency. Ufreq is a 16-bit unsigned number. The frequency calculation formula is: f=clk_sys/8/Ufreq. For example, if the system clock is clk_sys=3.579545MHz, Ufreq=8948, then the actual frequency measured is: f=3579545/8/8948=49.9908Hz. The voltage frequency measurement value is updated in a cycle of 0.64s (when the voltage frequency is 50Hz)/0.533s (when the voltage frequency is 60Hz).

Note: The zero-crossing detection of CSE7761 has a certain delay relative to the zero-crossing point of the actual signal: 2.2ms.

Table 2-2 Zero-crossing method

ZXD1	ZXD0	Zero Crossing Description
0	0	Indicates that the positive zero-crossing point is selected as the zero-crossing detection signal, and the zero-crossing output signal is the signal frequency/2
0	1	Indicates that the negative zero-crossing point is selected as the zero-crossing detection signal, and the zero-crossing output signal is the signal frequency/2
1	0	0 means that the ZX output changes at both the positive and negative zero crossing points, and the zero crossing output signal is the signal frequency.
1	1	Rate

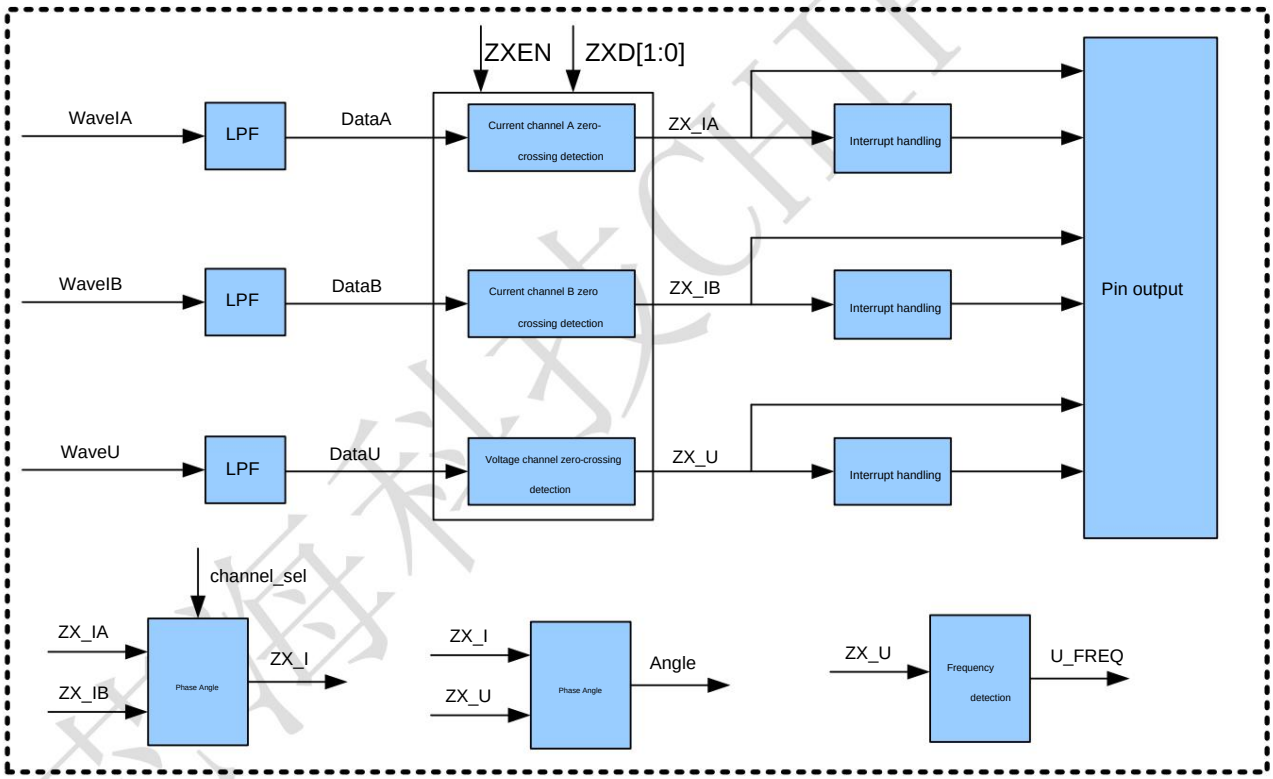


Figure 2-9 Zero-crossing detection block diagram

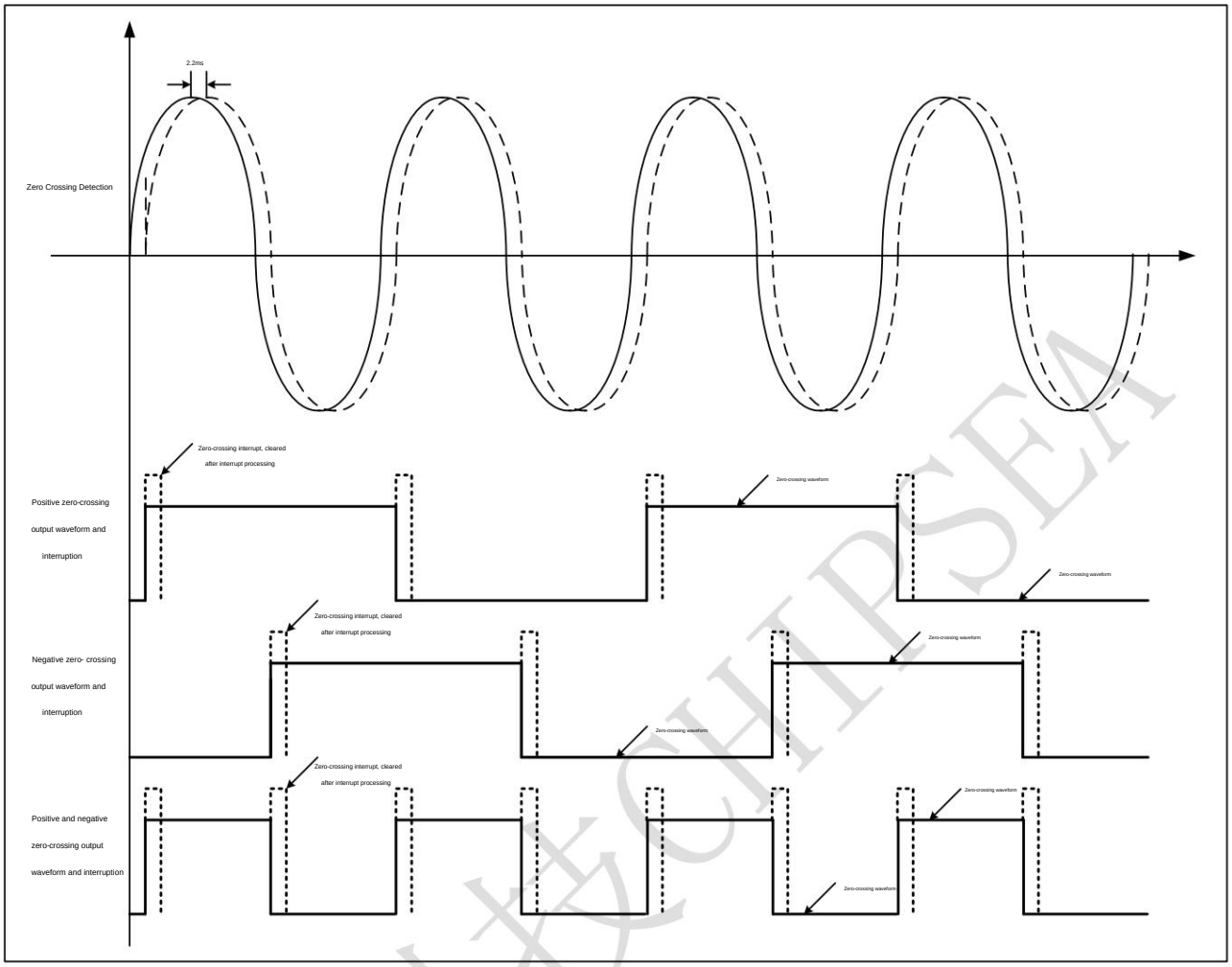


Figure 2-10 Zero-crossing waveform and zero-crossing interruption diagram

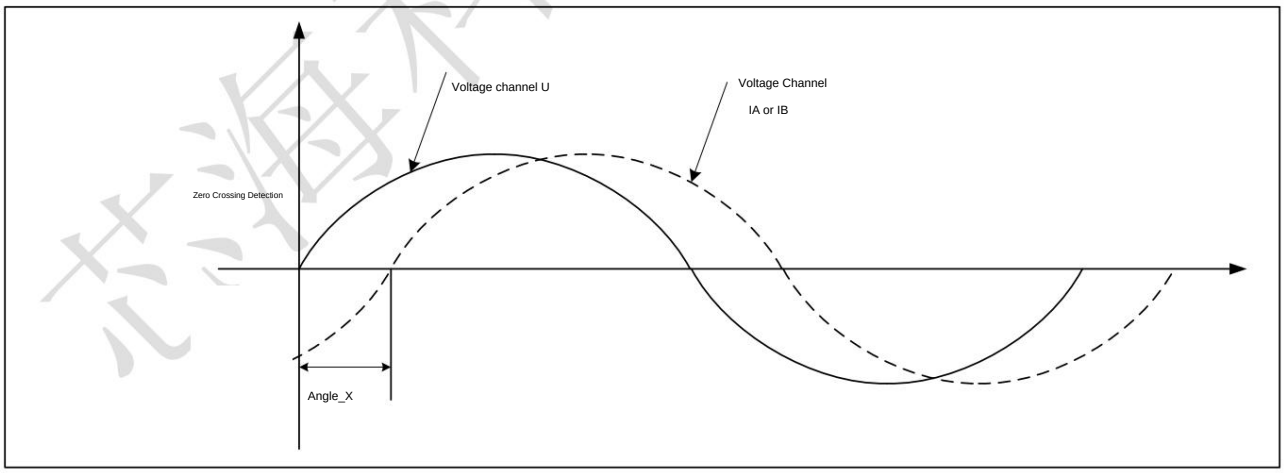


Figure 2-11 Phase angle diagram

2.10 Peak detection (turn on the instantaneous data function first)

The current channel A, current channel B and voltage channel of CSE7761 have peak detection characteristics. Peak detection can be enabled by configuring PeakEN.

Peak detection function (must be configured InstanEN = 1 first). This feature continuously records the maximum value of the voltage and current waveforms. Peak detection can

Used in conjunction with overvoltage and overcurrent detection, it provides a complete swell detection function (see Overcurrent and Overvoltage Detection).

Peak detection is the process of obtaining instantaneous measurements from the absolute values of the current and voltage output waveforms and storing them in three 24-bit registers.

The three registers for recording the peak values of current channel A, current channel B and voltage channel are PeakIA, PeakIB and PeakU respectively.

Whenever the absolute value of the waveform exceeds the value currently stored in the PeakIA, PeakIB, and PeakU registers, these registers are updated.

Reading these registers will clear the contents of the corresponding xPEAK registers and restart the peak measurement. This measurement has no associated time period. Note: After reading the peak register,

wait 10ms before reading the value of the peak register, otherwise the peak value read may not be the half-wave period.

The largest value in .

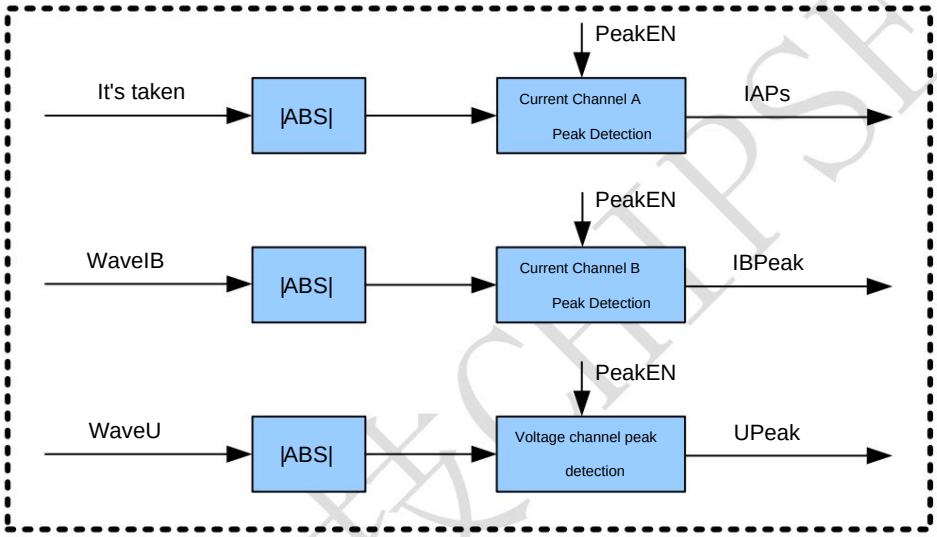


Figure 2-12 Peak detection block diagram

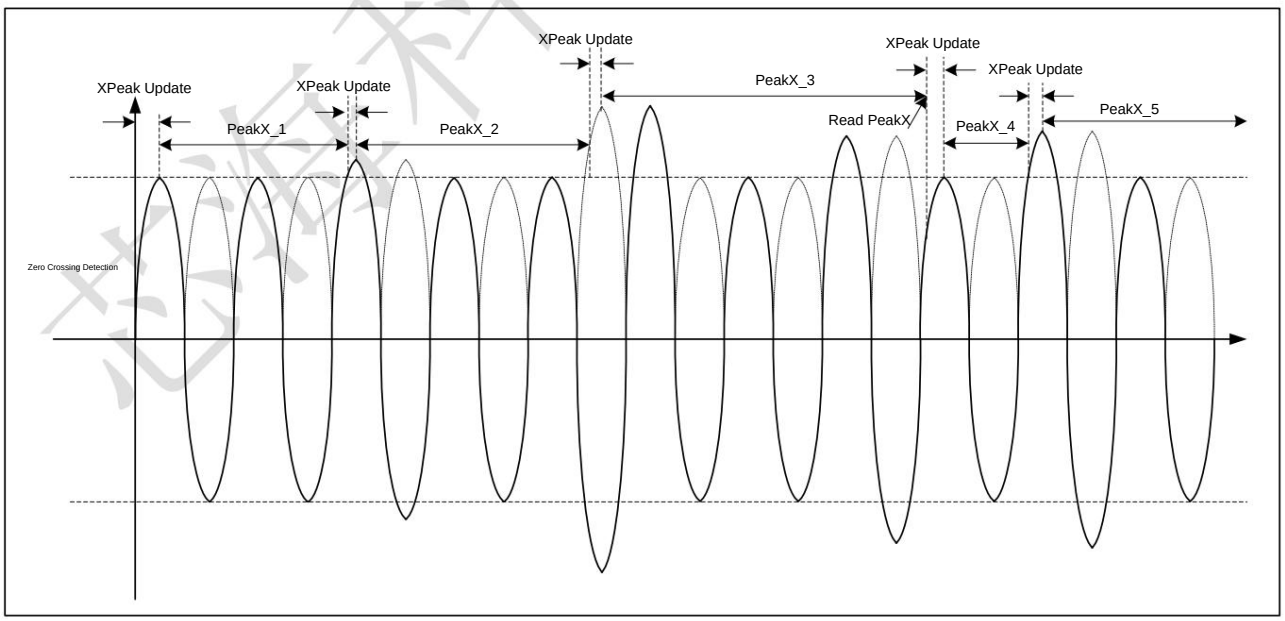


Figure 2-13 Peak detection diagram

2.11 Overcurrent, overvoltage, and active power overload detection (turn on the instantaneous data function first)

CSE7761 has over-current, over-voltage, and active power overload detection features. It can detect whether the absolute value of the current waveform, voltage waveform, and active power exceeds the programmable threshold. By configuring OVLVLEN, the over-current, over-voltage, and active power overload detection functions can be enabled (must be enabled). This feature uses instantaneous current, voltage signals and active power values.

There are four registers related to this feature: OVLVL, OIALVL, OIBLVL, OPLVL, which are used to set the voltage and current respectively. Channel A, current channel B, active power threshold, is an unsigned register, the default value of the register is 0xFFFF, and WaveIA, The high 17 bits of WaveIB, WaveU, and InstanP are aligned, and the operation method is {1'b0, LVL}-abs(Data[highest bit:highest bit-16]); by default, this feature is disabled. If CSE7761 detects overcurrent, overvoltage, or overpower conditions, OxIF/RoxIF will output the corresponding level. After reading RoxIF, the corresponding OxIF and RoxIF will be cleared to 0. If the corresponding interrupt enable signal is turned on, an output interrupt signal will be generated and output through IRQ.

There are two ways to calculate the overcurrent threshold of current channel A: apply actual current to calculate the overcurrent threshold or calculate the overcurrent threshold through a theoretical formula.

Example of calculating the overcurrent threshold of current channel A:

1. If 5A current is applied to current channel A, the value of the RmsIA register is RmsIA=0C49BAH (the average value of multiple consecutive readings). value), the overcurrent of current channel A is set to 10.5A; the OIALVL calculation formula is as follows:

   OIALVL=RmsIA/5*10.2*sqrt(2)/2^7=46E6Hÿ

   RmsIA/5*10.2: the register value of RmsIA at 10.2A; RmsIA/5*10.2*sqrt(2): the corresponding peak value at 10.2A; 2^7: shift the calculated result right by 7 bits.

2. The overcurrent threshold of current channel A can also be calculated directly by theoretical method:

   OIALVL=IA*R*1.5*PGAIA/Vref*2^16ÿ

   IA: The effective value of the overcurrent that needs to be set, in A.

   R: sampling resistor of current channel A, unit is ÿ; PGAIA: PGA amplification factor of current channel A, default is 16; Vref: chip reference voltage output, unit is V, typical value is 1.25V;

   *2^16: The register width of OIALVL is 16 bits;

It can be seen from the above calculation formula that applying the actual current to calculate the overcurrent threshold can eliminate the sampling resistor R, PGA amplification factor, The influence of chip reference Vref error. The calculation method of current channel B overcurrent threshold and voltage channel overvoltage threshold is similar to that of current channel A.

There are two ways to calculate the active power overload threshold: applying actual current and voltage to calculate the overload threshold or using a theoretical formula to calculate the overload threshold. Active power overload threshold, active power overload threshold calculation example:

1. If current and voltage are applied to current channel A, the power factor is 1, and the active power is 1000W, the value of the PowerPA register is PowerPA=2F23872H (the average value of multiple consecutive readings), and the active power overload is set to 10500W; the OPLVL calculation formula is as follows:

   OPLVL=PowerA/10500*1000/2^15=3AECHÿ

   PowerA/10500*1000: the register value of PowerPA when the power is 10500W; /2^15: shift the calculated result right by 15 bits.

2. The active power overload threshold can also be calculated directly by theoretical method:

   OPLVL=IA*Ria*U*Ru*2.25*PGAIA*PGAU/Vref^2*2^16ÿ

IA: The effective current value corresponding to the active overcurrent overload that needs to be set, in A.

IA: The voltage RMS value corresponding to the active overcurrent overload that needs to be set, in V.

Ria: sampling resistance of current channel A, in ÿ;

Ru: sampling resistance ratio of voltage channel, typical value is 1kÿ/(1Mÿ+1kÿ);

PGAIA: PGA gain of current channel A, the default is 16;

PGAU: PGA amplification factor of voltage channel, the default value is 1;

Vref: chip reference voltage output, unit is V, typical value is 1.25V;

*2^16: The register width of OPLVL is 16 bits;

From the above calculation formula, it can be seen that applying the actual current and voltage to calculate the active power overload threshold can eliminate the sampling resistor The influence of Ria/Ru, PGAIA and PGAU amplification factors, and chip reference Vref error.

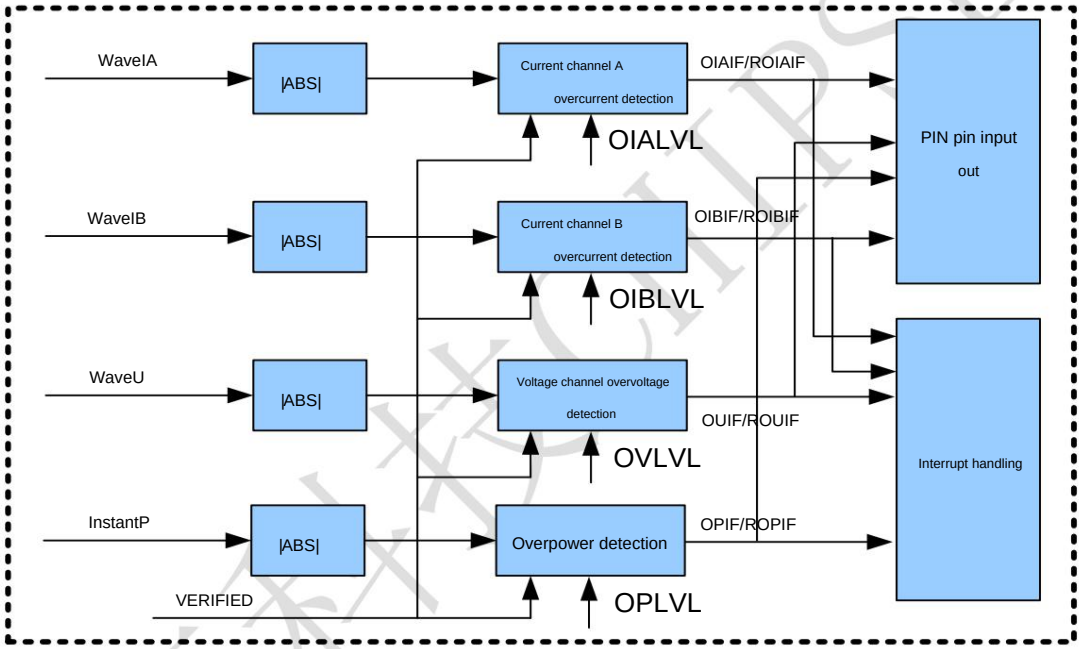


Figure 2-14 Overvoltage, overcurrent, and power overload detection block diagram

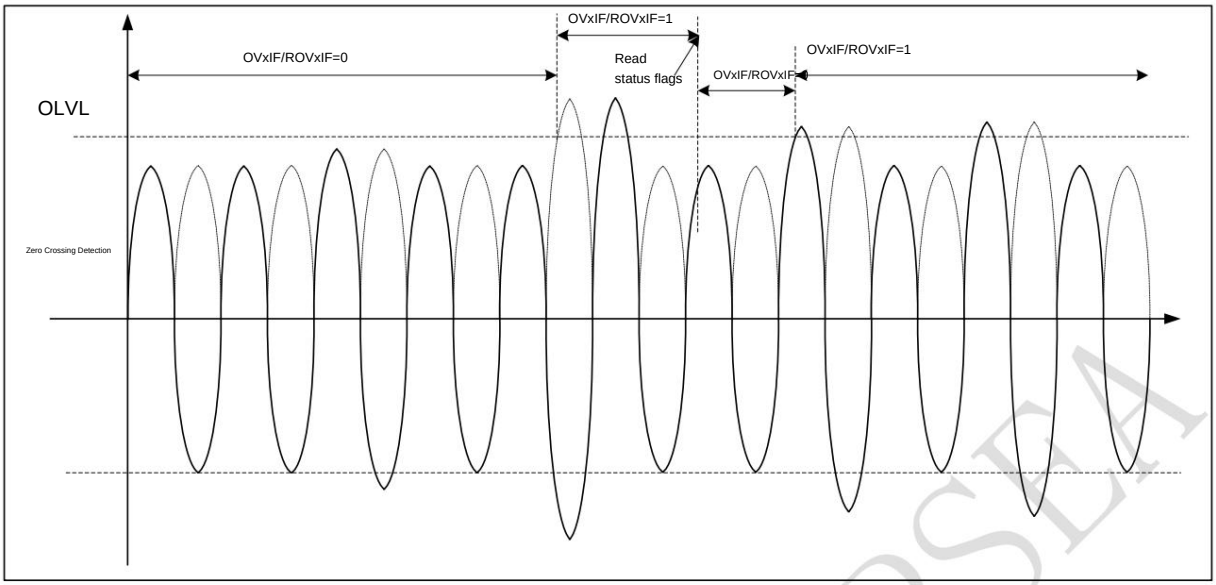


Figure 2-15 Schematic diagram of overvoltage, overcurrent and power overload detection

As shown in the figure, the active power overload detection method is the same as the voltage and current detection method, except that the power is a DC signal.

2.12 Voltage sag detection (turn on instantaneous data function first)

CSE7761 has a voltage sag detection feature. The voltage sag detection function can be enabled by configuring SAGEN (must be configured first).
InstanEN = 1), the user is alerted when the absolute value of the line voltage drops below a programmable threshold for a programmable number of line cycles.
This feature can provide an early warning signal of line voltage loss. The voltage sag feature is controlled by two registers: SAGCYC (unsigned) and
SAGLVL (unsigned). These registers control the sag period and sag voltage threshold, respectively. If a voltage sag occurs, the sag bit
SAG is set to 1 and will be cleared after being read.

Set the SAGCYC register:

The 16-bit unsigned SAGCYC register contains the programmable sag period, only the lower 8 bits are valid. The sag period refers to the number of half-wave cycles.
Below this number, the voltage channel must remain unchanged, and only when it exceeds or equals this number is it considered a sag condition.
1 LSB of the SAGCYC register corresponds to 1 half-wave cycle. The maximum value of the SAGCYC register is 255.

At 50 Hz, the longest dip cycle time is 2.55 seconds.

At 60 Hz, the longest dip cycle time is 2.125 seconds.

When this feature is enabled, if you change the SAGCYC value, the new SAGCYC period takes effect immediately.
Before writing a new period value to the SAGCYC register, the SAGLVL register should be set to zero to prevent overlap.
Reset to 0, effectively disabling this feature.

Set the SAGLVL register:

The 16-bit SAGLVL register contains the voltage amplitude value that the voltage channel must drop below for a sag event to occur.
Each LSB of the register is accurately mapped to the voltage channel peak register, so the amplitude can be set based on the peak reading of the voltage channel.
Set the SAGLVL register to apply the nominal voltage. Wait for a few line cycles, read the PeakU register to determine the voltage input, and then
This reading is then scaled to the magnitude required for sag detection. For example, if the sag threshold is required to be 80% of the nominal voltage, the peak value should be obtained.
The SAGLVL register is written with a value equal to 80% of the reading. This approach ensures accurate
SAGLVL value.

Voltage sag interruption:

The voltage sag detection feature of the CSE7761 has an associated interrupt SAGIF. If this interrupt is enabled, a voltage sag event will

The external IRQ pin goes low. This interrupt is disabled by default.

There are two ways to calculate the voltage channel undervoltage threshold: apply the actual voltage to calculate the undervoltage threshold or calculate the undervoltage threshold through a theoretical formula.

Example of calculating the voltage undervoltage threshold:

1. If 220V voltage is applied to the voltage channel, the value of the RmsU register is RmsU=21C21CH (the average value of multiple consecutive readings).

The voltage undervoltage setting is 220V*60%=132V; the SAGLVL calculation formula is as follows:

SAGLVL=RmsU/220*132*sqrt(2)/2^7=394AHÿ

RmsU/220*132: the register value of RmsU when the voltage is 132V;

RmsU/220*132*sqrt(2): the peak value corresponding to 132V;

2^7: shift the calculated result right by 7 bits.

2. The voltage channel undervoltage threshold can also be directly calculated theoretically:

SAGLVL=U*Ru*1.5*PGAU/Vref*2^16ÿ

U: voltage undervoltage effective value to be set, in V;

Ru: sampling resistance ratio of voltage channel, typical value is 1kÿ/(1Mÿ+1kÿ);

PGAU: PGA amplification factor of current channel A, the default value is 1;

Vref: chip reference voltage output, unit is V, typical value is 1.25V;

*2^16: The register width of SAGLVL is 16 bits;

From the above calculation formula, it can be seen that applying the actual current to calculate the overcurrent threshold can eliminate the sampling resistor Ru and PGAU amplification factor.

The influence of chip reference Vref error.

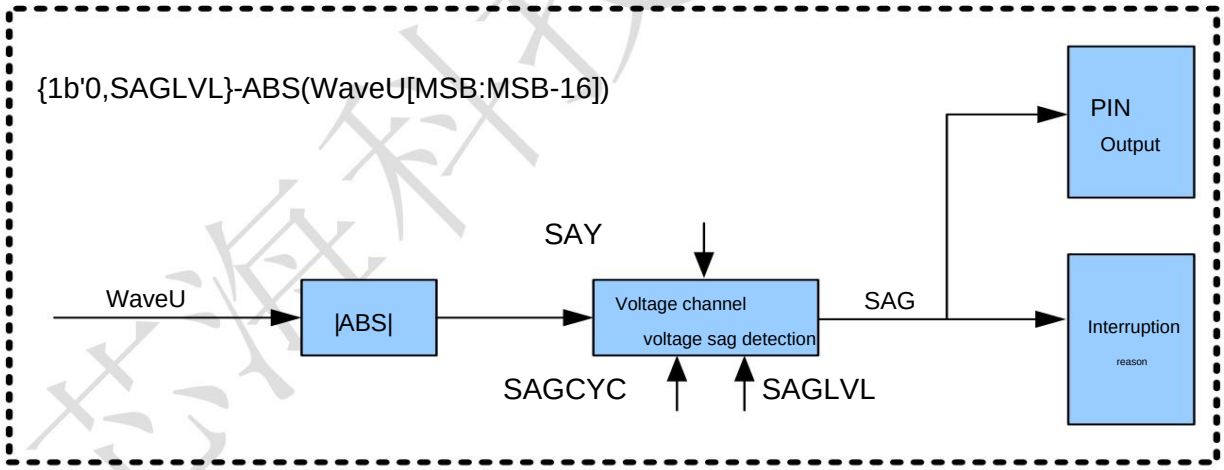


Figure 2-16 Voltage sag detection block diagram

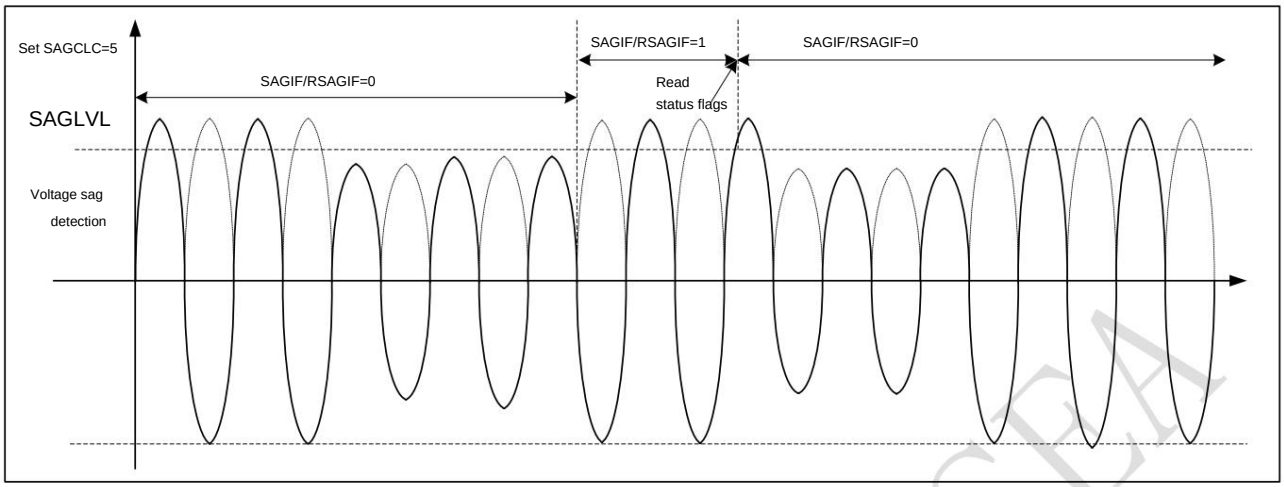


Figure 2-17 Schematic diagram of voltage sag detection

2.13 Mean Signal

CSE7761 provides average signals, including: current channel A RMS, current channel B RMS, voltage RMS,

Channel A active power, channel B active power, apparent power and power factor, except that the registers of active power and apparent power are 32 bits

All the average registers except the signed register are 24-bit signed registers. All measurement results are updated at the same rate.

Optional rates: 3.4Hz, 6.8Hz, 13.6Hz, 27.2Hz.

The CSE7761 provides an average interrupt status bit that allows measurements to be synchronized with the average signal update rate.

Will be cleared.

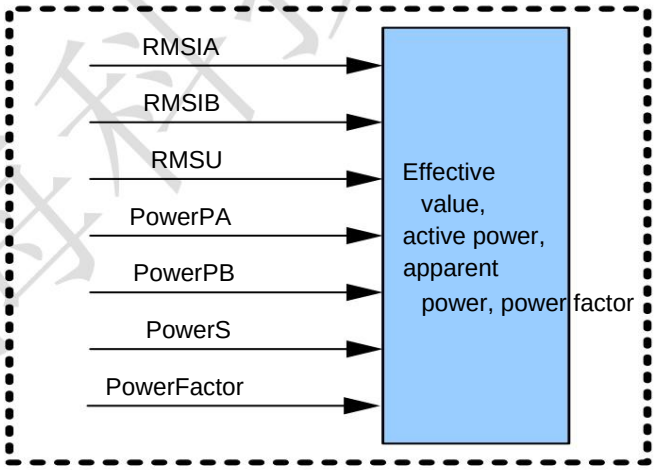


Figure 2-18 Mean data frame diagram

2.14 Transient Signal and Waveform Sampling

In addition to providing instantaneous voltage RMS, current RMS, active power, and apparent power (through configuration

INSTANEN can enable the instantaneous data output function). CSE7761 can also provide waveform data for voltage and current channels (by configuring

WAVEEN can be used to enable the transient data output function). This information can be used to analyze the transient data in more detail, including reconstructing the current and

Voltage input for harmonic analysis.

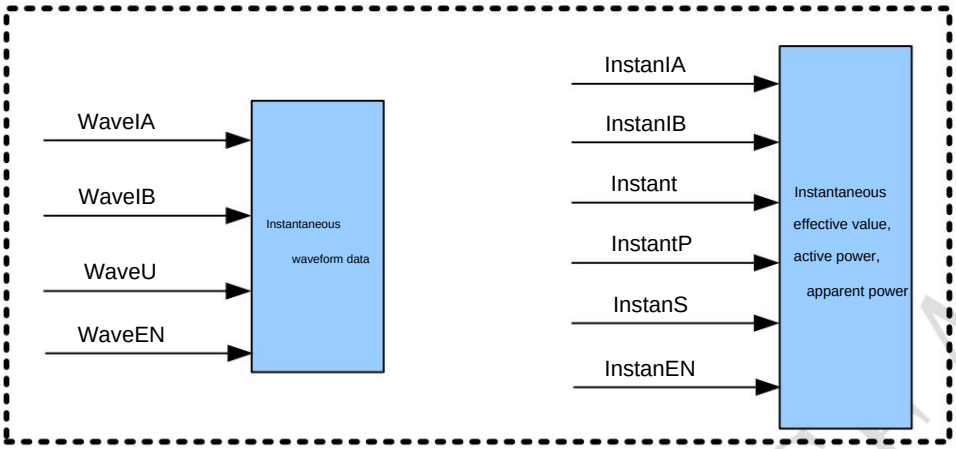


Figure 2-19 Transient signal and waveform data block diagram

The instantaneous voltage RMS, current RMS and instantaneous waveform data measurement results are provided through a set of 24-bit signed registers.

Active power and apparent power are provided in a set of 32-bit signed registers. All measurements are taken at a rate of 6.99 kHz (CLKIN/512).

renew.

The CSE7761 provides a transient interrupt status bit that triggers at a rate of 6.99 KHz, allowing measurements to be synchronized with the transient signal update rate.

The status bit will be cleared after it is read.

2.15 Temperature Sensor

CSE7761 current channel B also provides internal temperature detection, which can convert the voltage value output by the temperature sensor into a digital value through ADC and digital filtering.

The converted 24-bit AD value is stored in the RmsIB register.

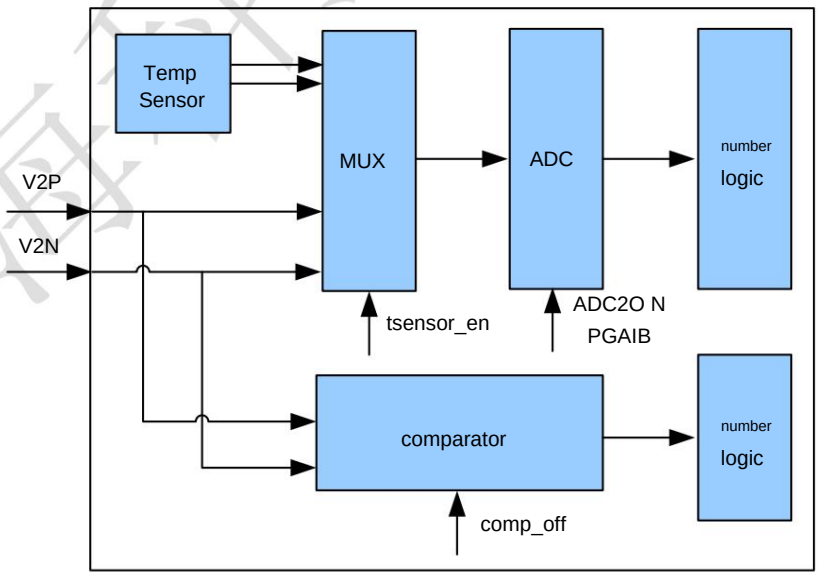


Figure 2-20 Temperature sensor measurement block diagram

The calibration steps of the CSE7761 temperature sensor are as follows:

1. Configure ADC2ON=1 (turn on B channel ADC), PGAIB[2:0]=000B; 2. Configure tensor_en=1 (turn on temperature measurement module), HPFIBOFF=1 (turn off B channel high pass filter); 3. Configure Tsensor_Step[1:0]=00B, read the RmsIB register value (it is recommended to read 4 times in a row for averaging), and record the register value is D1;

4. Configure Tsensor_Step[1:0]=01B, read the RmsIB register value (it is recommended to read 4 times in a row to get the average), and record the register value is D2;

5. Configure Tsensor_Step[1:0]=10B, read the RmsIB register value (it is recommended to read it 4 times in a row to get the average), and record the register value. is D3;

6. Configure Tsensor_Step[1:0]=11B, read the RmsIB register value (it is recommended to read it 4 times in a row to get the average), and record the register value is D4;

7. Add D1, D2, D3, and D4 and find the average to get D0: D0=(D1+D2+D3+D4)/4; Due to the change of process parameters, the temperature sensor needs to be calibrated. The calibration method is as follows:

Set the calibration temperature to Tc (unit: °C, e.g. 25 °C), the average value obtained from steps 3-7 is Dc, and save the Dc value in the storage unit. Then the temperature coefficient Tr = Dc/(273.15+Tc).

In actual use, according to steps 3-7, the average value D at the current temperature is obtained, and the current temperature is calculated according to the following formula (Unit: °C).

$$T = \frac{(+ 273.15) ÿ}{273.15}$$

2.16 Comparator

CSE7761 current channel B can also be used as the signal input of the comparator. When the peak-to-peak value of the input signal exceeds the value set by the internal comparator, threshold, the comparator will output a high level, and the comparator output signal comp_sign can be directly output through pulse1/pulse2 IO or through interruption.

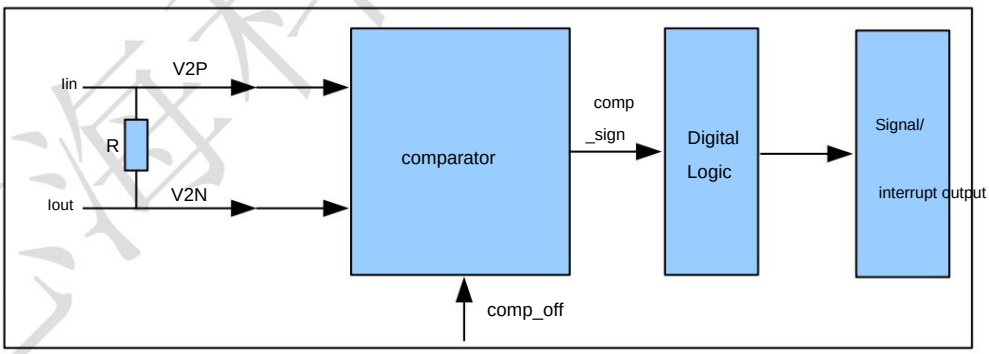


Figure 2-21 Comparator measurement block diagram

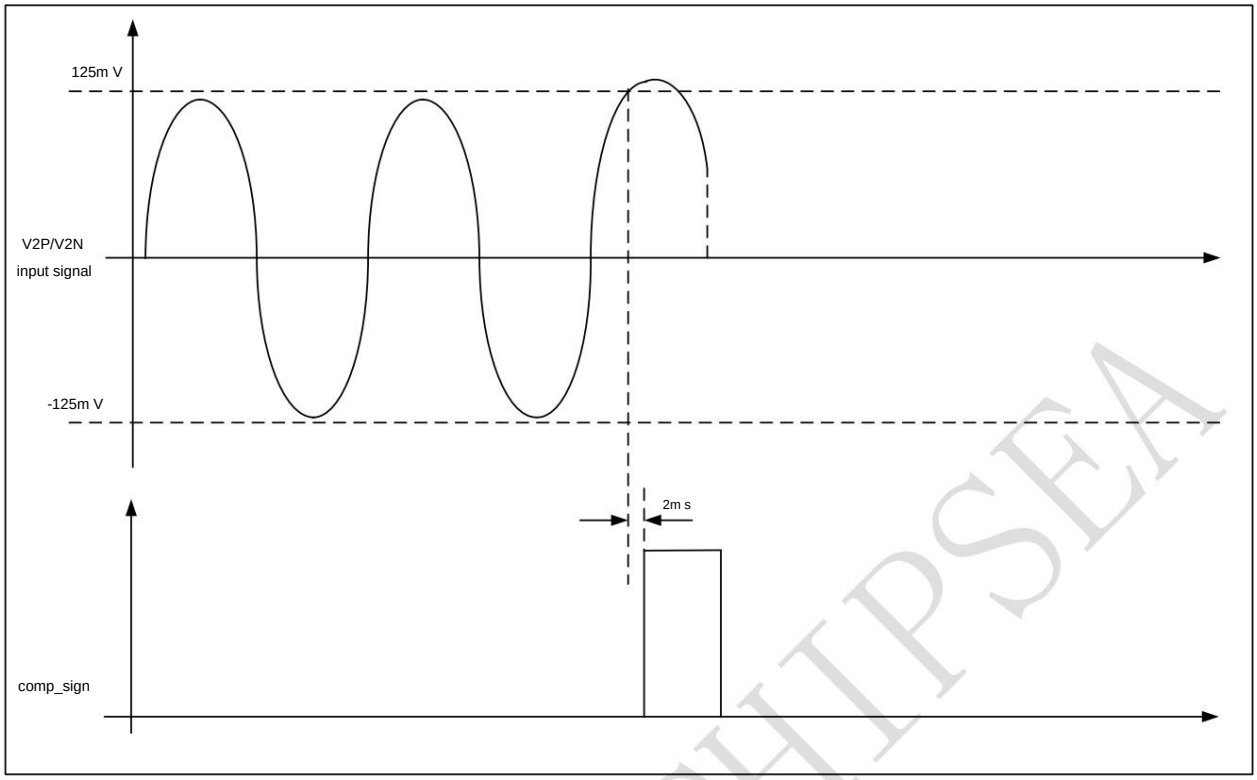


Figure 2-22 Comparator comp_sign output diagram

The steps to use the CSE7761 comparator are as follows:

1. Configure P1sel or P2sel = 010B, and output comp_sign through pulse1 or pluse2. 2. Configure comp_off = 1 (the comparator is in working state). When the comp_sign signal is detected to be high level, the external power supply needs to be disconnected, and CSE7761 needs to be powered on again to work normally.

3 Register Description

The CSE7761 register list is shown in the following table:

Table 3-1 CSE7761 register list

Address	Name	Word Length	Reset Value	Function	Write protection **R/W**
Description Calibration parameters and metering control registers					
00H	SYSCON	2	0A04h	System Control Registers	Yes R/W
01H	EMUCON	2	0000h	Metering Control Registers	Yes R/W
02H	HFConst	2	1000h	Pulse Frequency Registers	Yes R/W
03H	PstartPA	2	0060h	Channel A Active Starting Power Setting	Yes R/W
04H	PstartPB	2	0060h	Channel B Active Starting Power Setting	Yes R/W
05H	Food	2	0000h	Channel A Power Gain Calibration Register	Yes R/W
06H	PBGain	2	0000h	Channel B Power Gain Calibration Register	Yes R/W
07H	PhaseA	1	00h	Channel A Phase Calibration Register	Yes R/W
08H	Phase B.	1	00h	Channel B Phase Calibration Register	Yes R/W
0AH	HORRIBLE	2	0000h	Channel A Active Power Offset Calibration	Yes R/W
0BH	PBOS	2	0000h	Channel B Active Power Offset Calibration	Yes R/W
0EH	RmsIAOS	2	0000h	Current Channel A RMS Offset Compensation	Yes R/W
0FH	RmsIBOS	2	0000h	Current Channel B RMS Offset Compensation	Yes R/W
10H	IBGain	2	0000h	Current Channel B Gain Setting	Yes R/W
11H	PSGain	2	0000h	Apparent power gain calibration	Yes R/W
12H	PSOS	2	0000h	Apparent power Offset	Yes R/W
13H	EMUCON2	2	0001h	Compensation Metering	Yes R/W
17H	SAGCYC	2	0000h	control register 2 Voltage sag	Yes R/W
18H	SAGLVL	2	0000h	period setting Voltage sag threshold setting	Yes R/W
19H	OVLVL	2	FFFFh	Voltage overvoltage threshold setting	Yes R/W
1AH	OIALVL	2	FFFFh	Current channel A overcurrent threshold setting	Yes R/W
1BH	OIBLVL	2	FFFFh	Current channel B overcurrent threshold setting	Yes R/W
1CH	OPLVL	2	FFFFh	Active power overload threshold setting	Yes R/W
1DH	Pulse1SEL	2	3210h	PulseX pin output signal selection: X=1~2 Pulse1 outputs PFA by default Pulse2 outputs PFB by default	Yes R/W
Metering parameters and status registers					
20H	PFCnt_PA	2	0000h	Channel A fast combination active pulse counting	Yes R/W
21H	PFCnt_PB	2	0000h	Channel B fast combination active pulse counting	Yes R/W
22H	Angle	2	0000h	The phase angle between current and voltage is selected by command: The phase angle between current channel A and voltage channel or current channel B Phase angle with voltage channel	R
23H	Ufreq	2	0000h	Voltage	R
24H	RmsIA	3	000000h	frequency channel A Current effective value	R

25H	RmsIB	3	000000h	Channel B current effective value	·	R
26H	RmsU	3	000000h	Voltage RMS	·	R
27H PowerFactor		3	7FFFFFh	power factor register, selected by command: Channel A The power factor of channel A or the power factor of	·	R
28H	Energy_PA	3	000000h	channel B. The active energy of channel A is cleared after reading by default. Set to clear after reading	·	R
29H	Energy_PB	3	000000h	Channel B active energy, the default is clear after reading, configurable Set to not clear after	·	R
2CH	PowerPA	4	00000000h	reading Channel A active power, update rate 3.4Hz, 6.8Hzÿ13.6Hzÿ27.2Hz	·	R
2DH PowerPB		4	00000000h	Channel B active power, update rate 3.4Hz, 6.8Hz, 13.6Hz, 27.2Hz apparent power,	·	R
2EH	PowerS	4	00000000h	select channel A or channel B by command Apparent power, update rate 3.4Hz, 6.8Hz, 13.6Hzÿ27.2Hz	·	R
2FH EMU Status		3	00B32Fh	Metering Status and Checksum Registers	·	R
30H	PeakIA	3	000000h	Peak current of current channel A	·	R
31H	PeakIB	3	000000h	Peak voltage of channel B Peak	·	R
32H	PeakU	3	000000h	current of channel U Instantaneous	·	R
33H	InstanIA	3	000000h	value of current channel A	·	R
34H	InstanIB	3	000000h	Instantaneous value of current channel	·	R
35H	Instant	3	000000h	B Instantaneous value of voltage	·	R
36H	WaveIA	3	000000h	channel Instantaneous value of	·	R
37H	WaveIB	3	000000h	current channel A waveform Current channel B waveform	·	R
38H	WaveU	3	000000h	Voltage channel active	·	R
3CH	InstantP	4	00000000h	power instantaneous value, select channel A through command Or the instantaneous value of active power of channel B,	·	R
3DH	InstanS	4	00000000h	the instantaneous value of apparent power, select channel A through the command Or the instantaneous value of the actual power of	·	R
channel B, interrupt register						
40H	IE	2	0000h	Interrupt Enable Register	Yes R/W	
41H	IF	2	0000h	Interrupt flag register (not writable) Reset	·	R
42H	RIF	2	0000h	interrupt status register System	·	R
status register						
43H	SysStatus	1	-	System status register	·	R
44H	RDataEdit	4	-	Last SPI read data Last SPI write data	·	R
45H WDATA		2	-	Coefficient checksum Current channel	·	R
6FH Coeff_chksum		2	xxxxh	A RMS conversion	·	R
70H	RmsIAC	2	xxxxh	coefficient Current channel B RMS conversion	·	R
71H	RmsIBC	2	xxxxh	coefficient Voltage channel U RMS conversion	·	R
72H	RmsUC	2	xxxxh	coefficient Current channel A Active power	·	R
73H	PowerPAC	2	xxxxh	conversion coefficient	·	R

74H	PowerPBC	2	xxxxh	Current channel B Active power conversion factor	·	R
75H	PowerSC	2	xxxxh	Apparent power conversion factor	·	R
76H	EnergyAC	2	xxxxh	A channel energy conversion coefficient	·	R
77H	EnergyBC	2	xxxxh	B channel energy conversion coefficient	·	R
7FH	DeviceID	3	776110h	Chip ID	·	R
Note: For a write-protected register, you must first write a "write enable command" when writing input data to the register. The addresses not listed in the table are all 16-bit, cannot be written, and are read as 0 (the register with address 6EH is read as FFFFH);						

3.1 Calibration parameter register

3.1.1 System Control Register

SYSTEM Control Register (SYSCON) **Addr: 0x00H Default value: 0A04H**		
Bit	name	Functional Description
15-11	NC	-, default is 1
10	ADC2ON	=1, indicating that ADC current channel B is turned on =0, indicating that ADC current channel B is closed
9	NC	-, default is 1.
8-6	PGAIB[2:0]	Current channel B analog gain selection highest bit PGAIB[2:0]=1XX, PGA of current channel B=16 PGAIB[2:0]=011, PGA of current channel B=8 PGAIB[2:0]=010, PGA of current channel B=4 PGAIB[2:0]=001, PGA of current channel B=2 PGAIB[2:0]=000, PGA of current channel B=1
5-3	PGAU[2:0]	Voltage channel analog gain selection highest bit PGAU[2:0]=1XX, PGA of current channel U=16 PGAU[2:0]=011, PGA of current channel U=8 PGAU[2:0]=010, PGA of current channel U=4 PGAU[2:0]=001, PGA of current channel U=2 PGAU[2:0]=000, PGA of current channel U=1
2-0	PGAIA[2:0]	Current channel A analog gain selection highest bit PGAIA[2:0]=1XX, PGA of current channel A=16 PGAIA[2:0]=011, PGA of current channel A=8 PGAIA[2:0]=010, PGA of current channel A=4 PGAIA[2:0]=001, PGA of current channel A=2 PGAIA[2:0]=000, PGA of current channel A=1

3.1.2 Metering Control Register

Energy Measure Control Register (EMUCON) Addr: 0x01H Default value: 0000H		
Bit	name	Functional Description
15-14	Tsensor_Step[1:0]	Temperature Sensor measurement steps: =2'b00 The first step of temperature sensor measurement, the Offset of OP1 and OP2 is +/+. =2'b01 The second step of temperature sensor measurement, the offset of OP1 and OP2 is +/-. =2'b10 The third step of temperature sensor measurement, the Offset of OP1 and OP2 is -/+. =2'b11 The fourth step of temperature sensor measurement, the Offset of OP1 and OP2 is -/-. After measuring these four results, the AD value of the current measured temperature can be obtained by averaging them.

13	tensor_en	Temperature measurement module control =0, the temperature measurement module is turned off; =1, the temperature measurement module is turned on;
12	comp_off	Comparator module shutdown signal: =0 when the comparator module is in working state =1 when the comparator module is turned off
11-10	Pmode[1:0]	Active energy calculation method selection: Pmode = 00, both positive and negative active energy are accumulated, and the accumulation method is algebraic sum. The active power is indicated by the REVQ symbol; Pmode = 01, only accumulate positive active energy; Pmode = 10, both positive and negative active energy are accumulated, and the accumulation method is absolute value method. No reverse active power indication; Pmode = 11, reserved, the mode is the same as Pmode = 00
9	NC	-
8	ZXD1	The initial value of ZX output is 0, and different waveforms are output according to the configuration of ZXD1 and ZXD0: =0, indicating that the ZX output changes only at the selected zero crossing point =1, indicating that the ZX output changes at both positive and negative zero crossings
7	ZXD0	=0, indicating that the positive zero-crossing point is selected as the zero-crossing detection signal =1, indicating that the negative zero crossing point is selected as the zero crossing detection signal
6	HPFIBOFF	=0, enable current channel B digital high-pass filter =1, turn off the current channel B digital high-pass filter
5	HPFIAOFF	=0, enable current channel A digital high-pass filter =1, turn off the current channel A digital high-pass filter
4	HPFUOFF	=0, enable U channel digital high pass filter =1, turn off the U channel digital high pass filter
3-2	NC	-
1	PBRUN	PBRUN=1, enable PFB pulse output and active energy register accumulation; PBRUN=0 (default), turn off PFB pulse output and active energy register accumulation.
0	DESTROY	PARUN=1, enable PFA pulse output and active energy register accumulation; PARUN=0 (default), turn off PFA pulse output and active energy register accumulation.

3.1.3 Metering Control Register **2**

Energy Measure Control Register (EMUCON2) Addr: 0x13H Default value: 0001H		
Bit	name	Functional Description
15-13	NC	-
12	SDOCmos	=1, SDO pin CMOS open drain output =0, SDO pin CMOS output
11	EPB_CB	Energy_PB clear signal control, the default is 0, in UART mode, it needs to be configured as 1. UART mode does not support clear after read =1, Energy_PB will not be cleared after reading; =0, Energy_PB is cleared after reading;
10	EPA_CB	Energy_PA clear signal control, the default is 0, in UART mode, it needs to be configured as 1. UART mode does not support clear after read =1, Energy_PA will not be cleared after reading; =0, Energy_PA is cleared after reading;
9-8	DUPSEL[1:0]	Average register update frequency control DUPSEL update frequency DUPSEL update frequency

		00	3.4Hz	10	13.65Hz		
		01	6.8Hz	11	27.3Hz		
7	CHS_IB	Current channel B measurement selection signal =1, measure the current of channel B =0, measure the internal temperature of the chip					
6	PfactorEN	Power factor function enable =1, turn on the power factor output function =0, turn off the power factor output function					
5	WaveEN	Waveform data, instantaneous data output enable signal =1, turn on the waveform data output function =0, turn off the waveform data output function					
4	SAY	Voltage drop detection enable signal, need to configure WaveEN=1 first =1, turn on the voltage drop detection function =0, turn off the voltage drop detection function					
3	OverEN	Overvoltage, overcurrent, and overload detection enable signals. You need to configure WaveEN=1 first =1, turn on overvoltage, overcurrent and overload detection functions =0, turn off overvoltage, overcurrent and overload detection functions					
2	ZxEN	Zero-crossing detection, phase angle, voltage frequency measurement enable signal =1, turn on zero-crossing detection, phase angle, voltage-frequency measurement functions =0, turn off zero-crossing detection, phase angle, and voltage-frequency measurement functions					
1	PeakEN	Peak detection enable signal =1, turn on the peak detection function =0, turn off the peak detection function					
0	NC	Default is 1					

3.1.4 Pulse frequency register

HFConst	**Address: 0x02H Default value: 1000H**		
W/R	Bit15	Bit14……Bit1	Bit0

HFConst is a 16-bit unsigned number. When making a comparison, it is compared with the value of the fast pulse count register PFCNT. If the value of HFConst is equal to HFConst, there will be PF pulse output. Note: The maximum value of HFConst can only be 16'hfffd.

3.1.5 No-load active power (creep and start) threshold registers PstartPA, PstartPB

PstartPA	**Address: 0x03H Default value: 0060H**		
W/R	Bit15	Bit14……Bit1	Bit0

PstartPB	**Address: 0x04H Default value: 0060H**		
W/R	Bit15	Bit14……Bit1	Bit0

The no-load active power is configured by the PstartPA and PstartPB registers. PstartPA and PstartPB are 16-bit unsigned numbers. When the power is on, it is compared with the absolute value of the upper 24 bits of PowerPA and PowerPB (32-bit signed numbers) to make a start judgment; When |PowerP| is less than Pstart, it is considered as active creep. In the active creep state, PFA and PFB have no output and the energy register is not updated. (Energy_PA, Energy_PB), the power factor becomes 7FFFFF (PF = 1.0), but the two active power registers and the two current registers

The values of the device, voltage register, and apparent power register maintain normal output.

To increase sensitivity, this value can also be set to 50% of the starting power requirement specified by industry standards.

3.1.6 Active power and apparent power gain correction registers

Food	**Address: 0x05H Default value: 0000H**		
W/R	Bit15	14……1	Bit0

PBGain	**Address: 0x06H Default value: 0000H**		
W/R	Bit15	14……1	Bit0

PSGain	**Address: 0x11H Default value: 0000H**		
W/R	Bit15	14……1	Bit0

It includes three registers: PAGain, PBGain and PSGain, which are in binary complement format, with the highest bit being the sign bit.

PBGain is used for gain calibration of current channel A and active power of voltage channel; PBGain is used for gain calibration of current channel B and active power of voltage channel.

PSGain is used to select the gain calibration of the apparent power of the channel for measuring energy;

The calibration range of PAGain and PAGain is ±100%. The calibration range of PSGain is limited by PAGain or PBGain:

-100% <= PSGain+PAGain (when the channel is selected as current channel A) or PSGain+PBGain (when the channel is selected as current channel B)

For example, when PAGain=16'hFAFB, PSGain can be positively gained to 16'h7FFF as the maximum, and negatively gained to 16'h8505

is the minimum, when 16'h8504 will cause overflow.

Before calibration, the power value is P0, and after calibration, P1 = P0*(1+Gain/2^15).

For current channel A, Gain=PAGain;

For current channel B, Gain=PBGain;

For apparent power, Gain=PSGain+PAGain or PSGain+PBGain.

3.1.7 Phase Correction Register

PhaseA	**Address: 0x07H Default value: 00H**	
W/R	Bit7	Bit6…Bit0
	Sign bit	Data bits

Phase B.	**Address: 0x08H Default value: 00H**	
W/R	Bit7	Bit6…Bit0
	Sign bit	Data bits

PhaseA is the phase correction register for current channel A and voltage channel U, and PhaseB is the phase correction register for current channel B and voltage channel U.

Both registers are signed binary complement, where Bit7 is the sign bit. The phase calibration range at 50Hz is:

-2.575°~ +2.575°, phase calibration range at 60Hz: -3.09°~ +3.09°.

1 LSB represents a delay of 1/895KHz=1.12us/LSB. At 50Hz, 1 LSB represents 1.12us*360 degrees*50/10^6= 0.0201 degrees/LSB; at 60Hz, 1 LSB represents 1.12 us*360 degrees*60/10^6=0.0241 degrees/LSB.

3.1.8 Active power and apparent power **offset** correction register

HORRIBLE	Address: 0x0AH Default value: 0000H		
W/R	Bit15	14……1	Bit0

PBOS	Address: 0x0BH Default value: 0000H		
W/R	Bit15	14……1	Bit0

PSOS	Address: 0x12H Default value: 0000H		
W/R	Bit15	14……1	Bit0

Active offset calibration is suitable for precision calibration of small signals. All three registers are in binary complement format, with the highest bit being the sign bit.

The PAOS register is the active power offset calibration value of current channel A and U channel; the PBOS register is the active power offset calibration value of current channel B and U channel.

Active power Offset calibration value.

The PSOS register is the offset calibration value of the apparent power.

3.1.9 Current RMS **Offset** Correction Register

RmsIAOS	Address: 0x0EH Default value: 0000H		
W/R	Bit15	Bit14……Bit1	Bit0

RmsIBOS	Address: 0x0FH Default value: 0000H Write protection		
W/R	Bit15	Bit14……Bit1	Bit0

The RMS Offset calibration register is used to calibrate the accuracy of the current RMS small signal. Both registers are in binary complement format. The highest bit is the sign bit.

The RmsIAOS register is the current A rms value Offset calibration value, and the RmsIBOS register is the current B rms value Offset calibration value.

3.1.10 Current Channel **B** Gain Register

IBGain	Address: 0x10H Default value: 0000H		
W/R	Bit15	Bit14……Bit1	Bit0

The gain setting register of current channel B is used for consistency calibration of the two current channels. The consistency calibration is performed at 100% Ib. For usage, see the calibration method.

The channel B current gain register uses binary complement format, with the highest bit being the sign bit, and the calibration range is ±100%.

If IBGain>=2^15, then GainI2=(IBGain-2^16)/2^15, otherwise GainI2=IBGain/2^15.

Before correction, it is I2a; after correction, it is I2b. The relationship between the two is: I2b=I2a+I2a*GainI2.

3.1.11 Voltage sag setting register

SAGCYC	**Address: 0x17H Default value: 0000H**		
W/R	Bit15	Bit14……Bit1	Bit0

SAGLVL	**Address: 0x18H Default value: 0000H**		
W/R	Bit23	Bit22……Bit1	Bit0

The voltage sag feature is controlled by two registers: SAGCYC (unsigned number) and SAGLVL (unsigned number).

Control the sag period and sag voltage threshold.

3.1.12 Threshold Setting Register

OVLVL	**Address: 0x19H Default value: FFFFH**		
W/R	Bit15	Bit14……Bit1	Bit0

OIALVL	**Address: 0x1AH Default value: FFFFH**		
W/R	Bit15	Bit14……Bit1	Bit0

OIBLVL	**Address: 0x1BH** Default value: **FFFFH**		
W/R	Bit15	Bit14……Bit1	Bit0

OPLVL	**Address: 0x1CH** Default value: **FFFFH**		
W/R	Bit15	Bit14……Bit1	Bit0

OVLVL, OIALVL, OIBLVL, OPLVL, are used to set voltage, current channel A, current channel B, active power, respectively.

Overload threshold (channel A and channel B share a set of overload threshold registers), the register is an unsigned number, the default value is 0xFFFF; the default

In this case, this feature is disabled.

If the CSE7761 detects overcurrent, overvoltage, or overpower conditions, OVIF/ROVIFÿOIAIF/ROIAIFÿ

OIBIF/ROIBIF, OPIF/ROPIF will output corresponding levels.

3.1.13 PIN pin function output selection register

Pulse1SEL Addr: 0x1DH Default value: 3210H		
Bit	name	Functional Description
15-12	NC	NC, default value is 4'b0011
11-8	NC	NC, default value is 4'b0010
7-4	P2Sel	Pulse2 Pin output function selection, see the table below

3-0	P1Sel	Pulse1 Pin output function selection, see the table below

Table 3-2 Pulsex function output selection list

Pixel	Select Description
0000	Output of energy measurement calibration pulse PFA
0001	Output of energy measurement calibration pulse PFB
0010	Comparator indication signal comp_sign
0011	Interrupt signal IRQ output (default is high level, if it is an interrupt, set to 0)
0100	Power overload signal indication: Only PA or PB can be selected
0101	Channel A negative power indication signal
0110	Channel B negative power indication signal
0111	Instantaneous value update interrupt output
1000	Mean update interrupt output
1001	Voltage channel zero-crossing signal output
1010	Current channel A zero-crossing signal output
1011	Current channel B zero-crossing signal output
1100	Voltage channel overvoltage indication signal output
1101	Voltage channel undervoltage indication signal output
1110	Current channel A overcurrent signal indication output
1111	Current channel B overcurrent signal indication output

3.2 Metering parameter registers

3.2.1 Fast active energy pulse counter

PFCnt_PA	**Address: 0x20H Default value: 0000H**		
W/R	Bit15	14……1	Bit0

PFCnt_PB	**Address: 0x21H Default value: 0000H**		
W/R	Bit15	14……1	Bit0

PFCnt_PB Channel B fast active pulse count register; PFCnt_PA Channel A fast active pulse count register;

In order to prevent power loss during power on and off, the MCU reads back and saves the values of registers PFCnt_PA and PFCnt_PB when power is off. Then the MCU will rewrite these values into PFCnt_PA and PFCnt_PB when it is powered on next time.

When Prun=0, PFCnt_PB and PFCnt_PB stop updating and remain unchanged;

When Prun=1, when PFCnt_PB is equal to the value of HFConst, PFB will have a pulse output and the active energy register E_PB will be Add 1.

When PFCnt_PA is equal to the value of HFConst, PFA will have a pulse output and the active energy register E_PA will increase by 1.

3.2.2 Phase angle register

Angle	Address: 0x22H Default value: 0000H		
R	Bit15	14……1	Bit0

Angle represents the angle between the voltage channel and current channel A or between the voltage channel and current channel B. When the line frequency is 50Hz, the resolution is

When the line frequency is 60Hz, the resolution is 0.0965°.

3.2.3 Voltage-frequency register

Ufreq	Address: 0x23H Default value: 0000H		
R	Bit15	14……1	Bit0

It mainly measures the fundamental frequency Ufreq, with a measurement bandwidth of about 250Hz. The frequency value is a 16-bit unsigned number, and the parameter format is

The formula is: f=CLKI/8/Ufreq.

For example, if the system clock is CLKI=3.579545MHz and Ufreq=8948, then the actual frequency measured is:

f=3579545/8/8948=49.9908Hz.

The voltage-frequency measurement value is updated every 0.64s.

3.2.4 Current and voltage RMS registers

RmsIA	Address: 0x24H Default value: 000000H		
R	Bit23	22……1	Bit0

RmsIB	Address: 0x25H Default value: 000000H		
R	Bit23	22……1	Bit0

RmsU	Address: 0x26H Default value: 000000H		
R	Bit23	22……1	Bit0

The effective value of current and voltage Rms is a 24-bit signed number. The highest bit is 0 to indicate valid data, and the reading is treated as zero when the highest bit is 1.

The parameter update frequency can be selected from: 3.4Hz, 6.8Hz, 13.6Hz, 27.2Hz.

3.2.5 Power Factor Register

PF	Address: 0x27H Default value: 000000H		
R	Bit23	Bit22……Bit1	Bit0

PF is a 24-bit signed decimal, with the highest bit being the sign bit, obtained by dividing the active power by the apparent power. Power factor = sign bit

*[(PF22*2^-1)+ (PF21*2^-2)+……]; When PF=24'h7FFFFF, it means the power factor is 1.0; When PF=24'h800000,

Indicates that the power factor is -1.0; when PF=24'h400000, it indicates that the power factor is 0.5. The frequency of parameter update is 3.4Hz.

The following is 24'h7FFFFF;

3.2.6 Active Energy Register

E_PA	Address: 0x28H Default value: 000000H		
R	Bit23	22……1	Bit0

E_PB	Address: 0x29H Default value: 000000H		
R	Bit23	Bit22……Bit1	Bit0

E_PA and E_PB are power energy registers. E_PA is the energy register for channel A, and E_PB is the energy register for channel B.

When 0xFFFFFF overflows to 0x000000, overflow flags PEAOIF and PEBOIF will be generated (refer to IF 0x41H).

The electric energy parameter is an unsigned number. The register value of E_PA represents the accumulated number of PFA pulses, and the register value of E_PB represents the accumulated number of PFB pulses.

The energy represented by the smallest unit of the register is 1/EckWh. EC is the pulse constant.

When EPA_CB=0, the E_PA register is a read-clear type active energy register; when EPA_CB=1, the E_PA register is a read-clear type active energy register.

Active energy register that is not cleared afterwards;

When EPB_CB=0, the E_PB register is a read-clear type active energy register; when EPB_CB=1, the E_PB register is a read-clear type active energy register.

Active energy register that is not cleared afterwards;

3.2.7 Average Power Register

PowerA	Address: 0x2CH Default value: 00000000H		
R	Bit31	30……1	Bit0

PowerB	Address: 0x2DH Default value: 00000000H		
R	Bit31	30……1	Bit0

PowerS	Address: 0x2EH Default value: 00000000H		
R	Bit31	30……1	Bit0

The active power parameters PowerA/B and the apparent power parameters PowerS are both in binary complement format, 32-bit data, of which the highest bit is

Sign bit. The power parameter is updated at a frequency of 3.4 Hz.

PowerA is the average active power register of U channel and IA channel; PowerB is the average active power register of U channel and IB channel

Register; PowerS is the average active power of voltage channel U and current channel A or the average active power of voltage channel U and current channel B.

Power, determined by channel_sel;

3.2.8 Metering Status Register

EMU STATUS Register (EMUStatus) Addr: 0x2FH Default value: 00EF3BH		
Bit	name	Functional Description
23-22	NC	NC
21	Channel_sel	Current channel selection status flag. The default value is 0. =1 means that the current value is used to calculate the phase angle, apparent power, power factor, instantaneous active power, instantaneous The current channel of apparent power is current channel B; =0 means that the current value is used to calculate phase angle, apparent power, power factor, instantaneous active power, instantaneous The current channel of apparent power is current channel A; When ADC2ON=1, this bit is always 0.
20	NopldB When the active power of channel B is less than the starting power (0060H), NopldB is set to 1; otherwise, it is set to 0	
19	NopldA When the active power of channel A is less than the starting power, NopldA is set to 1; otherwise, it is set to 0	
18	REVPB	Channel B Reverse active power indication signal. When negative active power is detected, this signal When positive active power is detected again, the signal is 0. New value.
17	REVPA	Channel A Reverse active power indication signal. When negative active power is detected, this signal When positive active power is detected again, the signal is 0. New value.
16	ChksumBusy	Calibration data verification calculation status register. =0, indicating that the calibration data verification and calculation have been completed and the verification value is available. =1, indicating that the calibration data verification and calculation are not completed and the verification value is not available.
15—0	Chksum checksum output	

EMUStatus [15:0] is a register specially provided by CSE7761 to store the 16-bit calibration parameter configuration register.
The external MCU can detect this register to monitor whether the calibration data is disordered.

The checksum algorithm is to add two bytes and then invert them. For a single-byte register, expand it to a double-byte and then add it. The expanded bytes are 00H.

The register addresses of CSE7761 involved in checksum calculation are 00H-1FH. The checksum calculated according to the default value of CSE7761 is B32Ehÿ

In the following three cases, the checksum calculation is restarted: system reset, a write operation occurs to a register between 00H and 10H, 1FH A write operation occurs to a register and a read operation occurs to the EMUStatus register. One checksum calculation requires 2 system clock cycles.

3.2.9 Peak register

PeakIA	Address: 0x30H Default value: 000000H		
R	Bit23	Bit22……Bit1	Bit0

Peak value register of current channel A. The highest bit is the sign bit and is cleared after reading.

PeakIB	Address: 0x31H Default value: 000000H		
R	Bit23	Bit22……Bit1	Bit0

Peak value register of current channel B. The highest bit is the sign bit and is cleared after reading.

PeakU	Address: 0x32H Default value: 000000H		
R	Bit23	Bit22……Bit1	Bit0

Peak register of the voltage channel. The highest bit is the sign bit and is cleared after reading.

3.3 Instantaneous value and waveform registers

3.3.1 Instantaneous value register

InstanIA	Address: 0x33H Default value: 000000H		
R	Bit23	Bit22……Bit1	Bit0

The instantaneous value of the effective value of current channel A, the highest bit is the sign bit, and the update frequency is 6991Hz.

InstanIB	Address: 0x34H Default value: 000000H		
R	Bit23	Bit22……Bit1	Bit0

The instantaneous value of the effective value of current channel B, the highest bit is the sign bit, and the update frequency is 6991Hz.

Instant	Address: 0x35H Default value: 000000H		
R	Bit23	Bit22……Bit1	Bit0

The instantaneous value of the voltage channel U effective value, the highest bit is the sign bit, and the update frequency is 6991Hz.

InstantP	Address: 0x3CH Default value: 000000H		
R	Bit31	Bit30……Bit1	Bit0

Instantaneous value of active power, the highest bit is the sign bit, and the update frequency is 6991Hz.

InstanS	Address: 0x3DH Default value: 000000H		
R	Bit31	Bit30……Bit1	Bit0

Instantaneous value of apparent power, the highest bit is the sign bit, and the update frequency is 6991Hz

3.3.2 Waveform Register

WaveIA	Address: 0x36H Default value: 000000H		
R	Bit255	Bit254……Bit1	Bit0

The waveform data of current channel A after HPF, the highest bit is the sign bit, and the update frequency is 6991Hz.

WaveIB	Address: 0x37H Default value: 000000H		
R	Bit255	Bit254……Bit1	Bit0

The waveform data of current channel B after HPF, the highest bit is the sign bit, and the update frequency is 6991Hz.

WaveU	Address: 0x38H Default value: 000000H		
R	Bit255	Bit254……Bit1	Bit0

The waveform data of voltage channel U after HPF, the highest bit is the sign bit, and the update frequency is 6991Hz.

3.4 Interrupt Status Register

3.4.1 Interrupt Configuration and Enable Register **IE**

When the interrupt enable bit is configured as 1 and an interrupt occurs, the IRQ_N pin outputs a low level.

The write enable needs to be turned on.

Interrupt Enable Register (IE) Addr: 0x40H Default value: 0000H		
Bit	name	Functional Description
15	CompIE	Comparator interrupt enable
14	ZX_UIE	Voltage zero-crossing interrupt enable
13	ZX_IBIE	Current B zero-crossing interrupt enable
12	ZX_IAIE	Current A zero-crossing interrupt enable
11	SAGIE	Undervoltage interrupt enable
10	OPIE	Overpower interrupt enable
9	OVIE	Overvoltage interrupt enable
8	OIBIE	Current B overcurrent interrupt enable
7	OIAIE	Current A Overcurrent Interrupt Enable
6	INSTANIE	Instantaneous interrupt enable
5	reserve	
4	PEBOIE	Channel B active energy register overflow interrupt enable
3	PEAOIE	Channel A active energy register overflow interrupt enable
2	PFBIE	PFB interrupt enable
1	PFAIE	PFA interrupt enable
0	DUPDIE	Mean data update interrupt enable

3.4.2 Interrupt Status Register **IF**

Interrupt Enable Register (IF) Addr: 0x41H Default value: 0000H		
Bit	name	Functional Description
15	CompIF	=0, no comparator interrupt occurs =1, comparator interrupt occurs
14	ZX_UIF	=0, no voltage zero-crossing interruption occurs =1, voltage zero-crossing interrupt occurs
13	ZX_IBIF	=0, no current B zero-crossing interruption occurs =1, current B zero-crossing interrupt occurs
12	ZX_IAIF	=0, no current A zero-crossing interruption occurs =1, current A zero-crossing interrupt occurs
11	SAGIF	=0, no undervoltage interrupt occurs =1, voltage undervoltage interrupt occurs
10	OPIF	=0, no power overload interruption occurs =1, power overload interruption occurs

9	OVIF	=0, no overvoltage interruption occurs =1, overvoltage interrupt occurs
8	OIBIF	=0, no current B overcurrent interruption occurs =1, current B overcurrent interruption occurs
7	OIAIF	=0, no current A overcurrent interruption occurs =1, current A overcurrent interrupt occurs
6	INSTANIF	INSTANIF=0, no instantaneous value update event occurs; INSTANIF=1, an instantaneous value update event occurs;
5	NC	NC
4	PEBOIF	PEBOIF=0: Channel B has no active energy register overflow event; PEBOIF=1: channel B active energy register overflow event occurs;
3	PEAOIF	PEAOIF=0: Channel A has no active energy register overflow event; PEAOIF=1: channel A active energy register overflow event occurs;
2	PFBIF	PBFIF=0: PFB pulse output event does not occur; PBFIF=1: PFB pulse output event occurs;
1	PFBIF	PAFIF=0: PFA pulse output event does not occur; PAFIF=1: PFA pulse output event occurs;
0	DUPDIF	DUPDIF =0: no data update event occurs; DUPDIF =1: a data update event occurs.

IF is applicable to SPI interface and UART interface. When an interrupt event occurs, the hardware will set the corresponding interrupt flag to 1.

The generation of the IF interrupt flag is controlled by the interrupt enable register IE. After setting IE, the corresponding interrupt status register flag bit will be renew.

IF is a read-only register and is cleared to zero after reading.

3.4.3 Reset Interrupt Status Register **RIF**

Reset Interrupt Flag Register (RIF) Addr: 0x42H Default value: 0000H		
Bit	Name Function Description	
15	RCompIF	=0, no comparator interrupt occurs =1, comparator interrupt occurs
14	RZX_UIF	=0, no voltage zero-crossing interruption occurs =1, voltage zero-crossing interrupt occurs
13	RZX_IBIF	=0, no current B zero-crossing interruption occurs =1, current B zero-crossing interrupt occurs
12	RZX_IAIF	=0, no current A zero-crossing interruption occurs =1, current A zero-crossing interrupt occurs
11	RSAGIF	=0, no undervoltage interrupt occurs =1, voltage undervoltage interrupt occurs
10	ROPIF	=0, no power overload interruption occurs =1, power overload interruption occurs
9	ROVIF	=0, no overvoltage interruption occurs =1, overvoltage interrupt occurs
8	ROIBIF	=0, no current B overcurrent interruption occurs =1, current B overcurrent interruption occurs
7	ROIAIF = 0, no current A overcurrent interrupt occurs	

		=1, current A overcurrent interrupt occurs
6	RINSTANIF	=0, no instantaneous value update event occurs; =1, an instantaneous value update event occurs;
5	reserve	
4	RPEBOIF	=0: Channel B has no active energy register overflow event; =1: Channel B has an active energy register overflow event;
3	RPEAOIF	=0: Channel A has no active energy register overflow event; =1: Channel A has an active energy register overflow event;
2	RPFBIF	=0: PFB pulse output event did not occur; =1: PFB pulse output event occurred;
1	RPFAIF	=0: No PFA pulse output event occurs; =1: PFA pulse output event occurs;
0	RDUPDIF	=0: no data update event occurs; =1: data update event occurs.

For SPI and UART, the bit definition of RIF is the same as IF. When an interrupt event occurs, the corresponding interrupt flag is also set to 1.

Clear to 0, read RIF can clear both IF and RIF registers. RIF is the interrupt flag register that can still be received during the SPI/UART reading process.

Designed to accommodate new interrupts.

3.5 System Status Register

3.5.1 System Status Register **SysStatus**

System Status Register (SysStatus), Addressÿ 0x43HÿÿÿR		
Bit Name 7 Reserved		Functional Description
Read as 0.		
6	clksel	Chip system clock source indication signal =1, the chip is using the internal crystal oscillator; =0, the chip is using an external crystal oscillator;
5 Reserved Read as 0.		
4 WREN Write enable flag: =1 allows writing to write-protected registers; =0 does not allow writing to write-protected registers		
3 Reserved Read as 0.		
2 Reserved Read as 0.		
1 Reserved Read as 0.		
0	RST Reset flag. When the power-on reset ends and the software global reset is completed, this position is set to 1 and cleared after reading.	

3.5.2SPI read check register **RDATA**

RDataEdit	**Address: 0x44H Default value: 00000000H**		
R	Bit31	Bit30……Bit1	Bit0

The Rdata register stores the 4 bytes of data read last time and can be used for verification when reading data.

3.5.3SPI write check register **WDATA**

WDATA	**Address: 0x45H Default value: 0000H**		
R	Bit15	Bit`4……Bit1	Bit0

The Wdata register stores the 2 bytes of data written last time, which can be used for verification when writing data.

3.5.4 Coefficient Registers

Coeff_chksum	Address: 0x6FH		
RmsIAC	Address: 0x70H		
RmsIBC	Address: 0x71H		
RmsUC	Address: 0x72H		
PowerPAC	Address: 0x73H		
PowerPBC	Address: 0x74H		
PowerSC	Address: 0x75H		
EnergyAC	Address: 0x76H		
EnergyBC	Address: 0x77H		
W/R	Bit15	Bit14……Bit1	Bit0

The coefficient registers are all 16-bit unsigned numbers.

Coeff_chksum = ~ the lower 16 bits of (FFFFH+RmsIAC+.....+EnergyBC).

Calibration conditions of coefficients:

Chip operating voltage	**5V**	
Current Channel A	Input signal 5mV, PGA=16	The corresponding current effective value is 5A
Current Channel B	Input signal 5mV, PGA=16	The corresponding current effective value is 5A
Voltage Channel	Input signal 200mV, PGA=1	The corresponding voltage RMS is 200V
Active Power		The corresponding active power is 1000W
Apparent power		The corresponding apparent power is 1000W

Note: The chip coefficient calculation is realized by directly applying an AC voltage signal externally, without considering the use of resistors (current channel manganese The error of the coefficient is within ±1% due to the influence of copper resistance, voltage channel divider resistance) and other peripheral errors.

When the current channel sampling resistance is K1*1mÿ (K1 is the magnification/reduction factor, for example, the actual manganese copper is 2mÿ, K1=2; the actual manganese copper is 0.5mÿ, K1=0.5;), the voltage divider resistor ratio is K2*1Kÿ/1Mÿ (K2 is the magnification/reduction factor, for example, the voltage divider resistor The actual ratio is 2Kÿ/1Mÿ, K2=2; the actual voltage divider resistor ratio is 0.82Kÿ/1Mÿ, K2=0.82;) can be based on the following

The above formula is used for calculation:

Effective value calculation method:

$$\text{Current RMS} = \frac{\text{RmsXX*RmsXXC}}{\text{K1*2^23}}$$

$$\text{Voltage RMS} = \frac{\text{RmsU*RmsUC}}{\text{K2*2^22}}$$

RmsXX is the current/voltage RMS register value; RmsXXC is the current/voltage RMS coefficient register value;

The unit of the current effective value is mA (for example, 5000.1 represents 5.0001A); the unit of the voltage effective value is mA.

The bit is 10mV (if the calculated value is 22008.1, it represents 220.081V);

Active power/apparent power calculation method:

$$\text{power/Apparent power} = \frac{\text{PowerXX*PowerXXC Active}}{\text{K1*K2*2^31}}$$

PowerXX is the register value of active power/apparent power; RmsXXC is the register value of current/voltage effective value coefficient;

The unit of active power/apparent power calculation is W (for example, if the calculated value is 1100.1, it means 1100.1W);

Active energy calculation method:

$$\text{energy} = \frac{\text{EnergyXX*EnergyXC*HFConst Electric}}{\text{K1*K2*2^29*4096}} * 1000$$

EnergyXX is the energy pulse register value; EnergyXXC is the energy pulse calibration coefficient register value;

The unit of electric energy calculation is KW*h(kWh) (e.g. the calculated value is 2.101, which means 2.101 kWh);

3.5.5DeviceID Register

DeviceID	**Address: 0x7FH Default value: 776110H**		
R	Bit23	Bit22……Bit1	Bit0

This register has a fixed value of 776110H.

4. Calibration Method

4.1 Overview

CSE7761 can realize software calibration. The active power accuracy of the calibrated meter can reach 0.5s level. The calibration methods of CSE7761 include:

ÿ Adjustable meter constant (HFConst) ÿ Provide

phase calibration for A/B channels

ÿ Provide current gain calibration for channel B

ÿ Provide active gain calibration for A/B channels ÿ Provide active

offset calibration for A/B channels ÿ Provide effective value offset

calibration for A/B channels ÿ Provide gain calibration and offset calibration

for apparent power ÿ Provide automatic calibration data verification function

4.2 Calibration process and parameter calculation

When calibrating the single-phase LCD meter designed by CSE7761, a standard electric energy meter must be provided. When calibrating the meter using a standard electric energy meter, the active energy pulse PFA/PFB can be directly connected to the standard meter through an optical coupler, and then the error reading of the standard electric energy meter can be used to calibrate the meter. CSE7761 is calibrated.

4.2.1 Calibration process

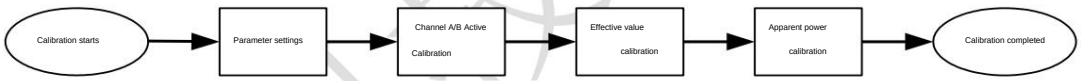


Figure 4-1 Calibration process

4.2.2 Parameter settings

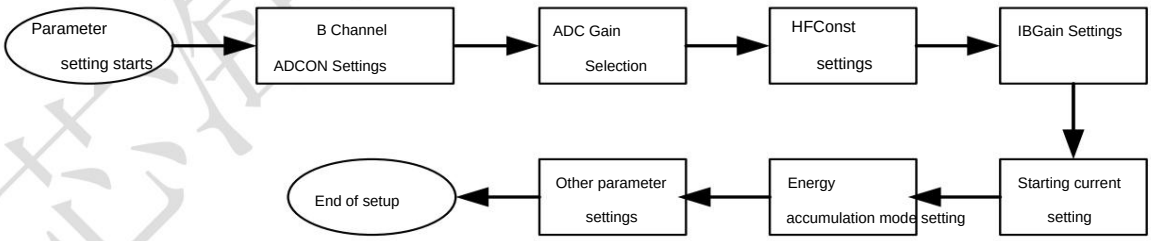


Figure 4-2 Parameter setting process

HFConst parameter calculation:

The calculation formula of HFConst (calculated based on the current size of channel A):

$$HFConst = 23.2*10^{11}* EC\ One\ Ib \quad \frac{*\ See\ you\ later}{* \quad *}$$

Vu: voltage of the voltage channel when rated voltage is input (voltage on the pin × amplification factor: 1, 2, 4, 8, 16);

Vi: Voltage of the current channel when rated current is input (voltage on the pin × amplification factor: 1, 2, 4, 8, 16); Un: Rated input voltage; Ib: Rated input current; EC:

Pulse constant.

Calculation of IBGain:

ÿIBGain = (IA-IB) / IB. If ÿIBGain

ÿ 0, then IBGain = INT [ÿIBGain × 2 15]; otherwise ÿIBGain < 0, then IBGain = INT

[2 16 + ÿIBGain × 2 15]; IA: The effective current value of current channel A (RmsIA register value); IB: The effective current value of current channel B (RmsIB register value).

4.2.3 Active power calibration

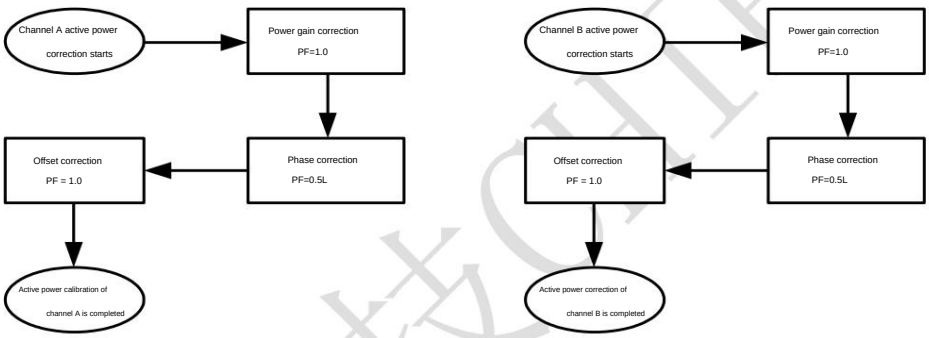


Figure 4-3 Active power calibration process

1. The power gain calibration of channel A can be achieved by configuring the PAGain register. The calculation method of PAGain is as follows:

If the standard meter reads an error of err on channel A at 100% Ib and PF=1:

ÿPAGain=-err/(1+err).

If ÿPAGain ÿ 0, then PAGain = INT[ÿPAGain ×2 15]; otherwise, if ÿPAGain < 0, then

PAGain = INT[2 ^{16} +ÿPAGain ×2 15]ÿ

The power gain calibration of channel B can be achieved by configuring the PBGain register in the same way as PAGain.

2. Calculation method of phase calibration register of A/B channel: If

the standard meter reads the error err on A/B channel, 100% Ib, PF=0.5L, then the phase compensation formula is:

ÿ=arcsin(-err/sqrt(3)) *180/3.14159. Or ÿ=arccos((err+1)/

2)*180/3.14159- 60 degrees for 50Hz, PhaseA/B has a relationship

of 0.02 degrees/LSB, so we have

If ÿ>=0, PhaseA/B = INT[ÿ/0.02]. If ÿ<0, PhaseA/B =

INT[2^8+ÿ/0.02]. 3. Active power offset calibration is an effective

means to improve the small signal active power accuracy when the external noise (PCB noise, transformer noise, etc.) is large and the integrated energy affects the small signal accuracy. If the external noise has little effect on the small signal active power accuracy, this step can be ignored.

If the standard meter applies Un to the energy meter, channel A has 5% Ib, and PF = 1, the read error is err, and the value of the PowerA register is

PA (the average value of 16 consecutive readings, the refresh frequency of PowerA is about 3.4Hz), then the value calculation process of the PAOS register is as follows:

PAOS = INT[-(PA×err)]; The calculation process

of PBOS register is the same.

4.2.4 Effective value calibration

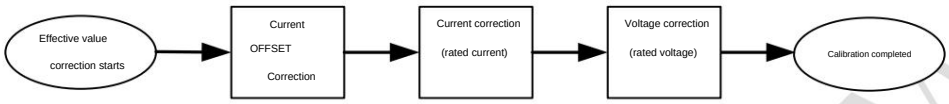


Figure 4-4 Effective value calibration process

1. Current offset calibration can improve the accuracy of small signal current RMS value

RmsIAOS register calculation process:

1) Configure the standard meter, make U=Un, current channel input Vi=0; 2) Wait for the DUPDIF flag

to update (refresh at about 3.4Hz per second); 3) MCU takes the RmsIA register value and stores it

temporarily; 4) Repeat steps 2 and 3 11 times, ignore the first data, take

the next 10 data and average to get Iave[23:0]; 5) Invert Iave bit by bit (including the sign bit) and add 1, take the sign bit and fill it into Bit15 of the RmsIAOS

register, take Bit14~Bit0 and fill it into RmsIAOS Bit14~Bit0 to get RmsIAOS;

6) The effective value Offset calibration is completed.

The RmsIBOS calibration formula and RmsIAOS register calculation process are the same. 2. After calibrating the

current Offset, calibrate the A/B channel current conversion coefficient KiA/KiB and the voltage conversion coefficient Ku.

This step is completed by MCU, and the calculation process is as follows:

If the RmsIA register reading is RmsIAreg at rated current Ib, then KiAÿIb/RmsIAreg, where KiA is the ratio of the rated value to the

corresponding register at rated input.

The calculation process of the B channel conversion coefficient KiB is the same as that of the voltage conversion coefficient Ku.

4.2.5 Apparent power calibration

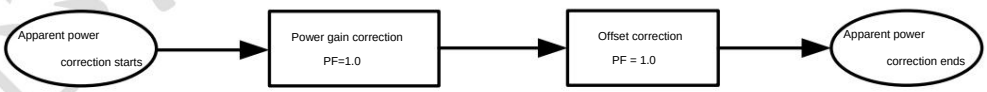


Figure 4-5 Apparent power calibration process

1. Apparent power gain calibration can be achieved by configuring the PSGain register. The calculation method of PSGain is as follows:

If the channel for measuring energy is channel A, when the standard meter applies Un to the energy meter, channel A is 100% Ib, and PF=1, the A channel is read.

The average active power register value of the channel is PowerPA, and the average apparent power register value is PowerS:

ÿPSGain=(PowerPA-PowerS)/PowerS. If ÿPSGain ÿ 0, then PSGain =

INT[ÿPSGain ×215];

Otherwise, ÿPSGain < 0, then PSGain = INT[2^16 +ÿPSGain ×215];

2. Apparent Offset calibration helps improve the accuracy of power factor when the signal is small. If

the channel for measuring energy is channel A, when the standard meter applies Un to the energy meter, channel A has 5% Ib, and PF=1, the average active power register value of channel A is read as PowerPA, and the average apparent power register value is PowerS. Then the calculation process of the PSOS register value is as follows:

PSOS = INT[PowerPA-PowerS]ÿ

4.2.6 Examples

Assume that a sample meter with a rated input of 220V (Un), 10A (Ib), and a pulse constant of 1200imp/kWh (EC) is designed. The A channel current uses 250μÿ manganese copper, the channel A analog channel gain is 16 times, the B channel current sampling uses a current transformer, and the B channel gain is selected to be 1 times. The voltage sampling uses a resistor divider input, the analog channel gain is 1 times, and the chip pin value is 0.16V.

1: Calculate HFConst

Vu=0.16V, Vi=10×0.00025×16=0.040V, EC=1200imp/kWh, Un=220V, Ib=10A.

HFConstÿINT[23.196×Vu×Vi×1011/(EC×Un×Ib)]=5623=15F7H, after rounding, HFConst is 15F7H.

Write this value into the HFConst register to complete the HFConst calibration.

2: Active calibration of channel A

2.1 A channel power gain calibration

The power source outputs 220V 10A with a power factor of 1.0, and the standard meter shows an error of 1.2%, then:

ÿPAGain = -0.012/(1+0.012)=-0.01186,ÿPAGainÿ0, PAGain=INT[216+ÿPAGain ×215]=-0.01186 ×215+216=0xFE7BH, write FE7BH into the PAGain register to complete the A channel gain calibration.

2.2 A channel phase calibration

After calibrating the resistive gain, change the power factor to 0.5L. The error displayed by the standard meter is -0.4%, so ÿ>0, PhaseA =INT[ÿ/0.02]=(arcsin(-(-0.004)/sqrt(3)))/0.02=7, input 07H to PhaseA register to complete phase calibration of channel A; if the error displayed by the standard table is -0.4%, then ÿ>0, PhaseA =INT[ÿ/0.02]=(arcsin(-(0.004)/sqrt(3)))/0.02=-7, when the phase selection bit Phase_sel=0, input (2^8-7-96)=99H to PhaseA register; when Phase_sel=1, input (2^8-7)=F9H to PhaseA register;

2.3 A channel offset calibration

If the standard meter applies Un to the energy meter, channel A has 5% Ib, and PF=1, the read error is err=0.3%, and the value of the PowerA register is If PA=000F5AB7H (the average value of 16 consecutive reads, the refresh frequency of PowerA is about 3.4Hz), then the value of the PAOS register is PAOS = INT[-(000F5AB7H×0.3%)]=F436Hÿ

The active calibration of channel B is similar to that of channel A.

3: Effective value calibration

The chip provides a current RMS offset calibration register. When the current input is 0, the current RMS register value is 268H (can be read several times to get the average value), take the inverse and add 1 to get FFFD98, take the sign bit and fill it into Bit15 of the RmsIAOS register, take Bit14~Bit0 and fill it into PAOS Bit14~Bit0 to get FD98H, write it into the RmsIAOS register, and complete the A channel effective value calibration.

The calibration of channel B is similar to that of channel A.

4: Apparent power calibration

4.1 Apparent power gain calibration

Assuming that the channel for measuring energy is channel A, when the standard meter applies Un to the energy meter, channel A is 100% Ib, and PF=1, the A reading is: The average active power register value of the channel is PowerPA = 00AF389AH, and the average apparent power register value is PowerS = 00AE04D4H. Then the calculation process of the PSGAIN register value is as follows:

ÿPSGain=(PowerPA -PowerS)/ PowerS =0.691%ÿ

PSGain =INT[ÿPSGain ×215]=226=00E2Hÿ

4.2 Apparent Power Offset Calibration

Assuming that the channel for measuring energy is channel A, when the standard meter applies Un to the energy meter, channel A 5% Ib, PF = 1, read the channel A. The average active power register value of the channel is PowerPA = 0008C2D4H, and the average apparent power register value is PowerS = 0008C1D7H.

The value calculation process of the PSOS register is as follows:

PSOS = INT[PowerPA -PowerS]=253=00FDHÿ

5. Communication Interface

5.1 SPI Interface

5.1.1CSE7761 SPI command format

When the SPIEN pin of the CSE7761 chip is connected to a high level, the communication mode of the CSE7761 is SPI.

5.1.2SPI command format

SPI is a four-wire system: SCSN, SDI, SDO and SCLK, including a read register RDATA and a write register WDATA.

All data transmission operations are synchronized with SLCK. CSE7761 outputs data from SDO pin on the rising edge and from SDI pin on the falling edge.

Read data. During the period when SCSN is low, the register can be read and written continuously. During SPI operation, if two SCLKs are on

When the rising edge exceeds 9.15ms (2^15 of the system clock), the SPI module is reset (ie, the minimum SPI rate is 109.25Hz).

The SPI command register is an 8-bit wide register. For read and write operations, bit 7 of the command register is used to determine the current data transfer.

The type of input operation is read or write operation, and bit6-0 of the command register is the address of the register to be read or written.

Bit7-0 of the command register is fixed to 0xEA.

Table 5-1 CSE7761 SPI command list

Command Name	Command Register	data	describe
Read command {0,REG_ADR[6:0]} RDATA			Read data from the register at address REG_ADR[6:0]. Note: Reading an invalid address will return a value of 00h
Write command {1,REG_ADR[6:0]} WDATA	Write data to the register at address REG_ADR[6:0]		
Write enable command	0xEA	0xE5	Enable write operation
Write protection command	0xEA	0xDC	Disable write operation
Current Channel A choose	0xEA	0x5A	Current channel A setting command, specifies the current used to calculate the apparent power, Power factor, phase angle, instantaneous active power, instantaneous apparent power and The channel for the active power overload signal indication is channel A.
Current Channel B choose	0xEA	0xA5	Current channel B setting command, specifies the current used to calculate the apparent power, Power factor, phase angle, instantaneous active power, instantaneous apparent power and The channel for the power overload signal indication is channel B
Reset instruction	0xEA	0x96	Reset instruction. After receiving the instruction, the chip is reset.

5.1.3SPI write operation timing

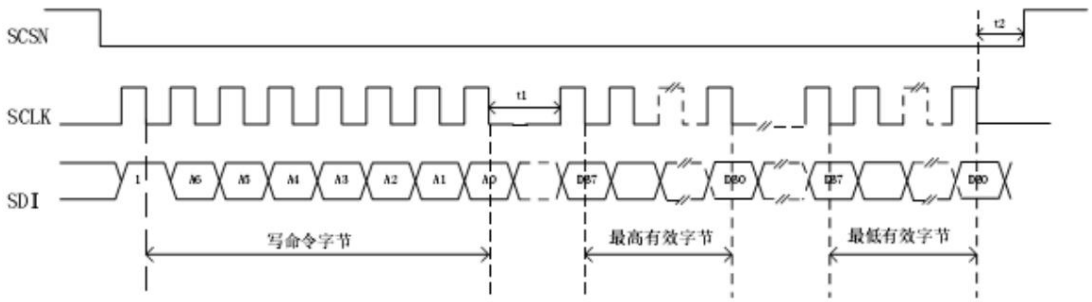


Figure 5-1 SPI write operation timing

Working process:

1. After SCSN is valid, the host first writes the command byte through SPI, and then writes the data byte. Note:

2. Transmit in bytes, with high bits first and low bits last; 3. For multi-byte registers, high

byte content is transmitted first, then low byte content; 4. The host writes data on the rising edge of SCLK,

and the slave reads data on the falling edge of SCLK;

5. The time t1 between data bytes must be greater than or equal to half of the SCLK cycle;

6. The LSB of the last byte is transmitted, and SCSN changes from low to high to end the data transmission.

The time t2 between them should be greater than or equal to half of the SCLK cycle.

Note: Registers with write protection function must be written with a write enable command before writing operations.

5.1.4SPI read operation timing

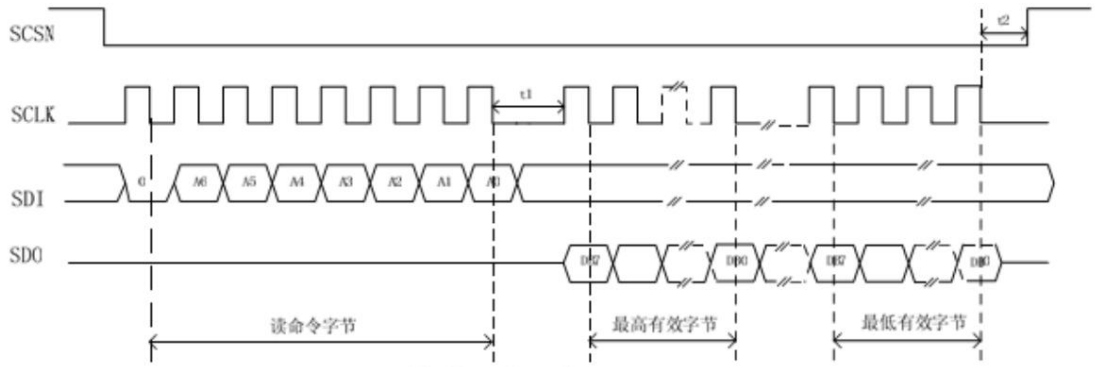


Figure 5-2 SPI read operation timing

Working process:

After SCSN is valid, the switchboard first writes the command byte through SPI. After receiving the read command, the slave sends the data on the rising edge of SCLK.

Output from SDO pin bit by bit.

1. Transmitted in bytes, with high bits first and low bits last;

2. For multi-byte registers, the high byte content is output first, and then the low byte content is transmitted;

3. The host transmits the command byte at the rising edge of SCLK, and the slave outputs the data from SDO at the rising edge of SCLK; 4.

The time t1 of the data byte must be greater than or equal to half the SCLK time;

5. The LSB of the last byte is transmitted, and SCSN changes from low to high to end the data transmission.

The time t2 between them should be greater than or equal to half of the SCLK cycle.

5.2 CSE7761 UART command format

5.2.1UART communication format

Works in slave mode, half-duplex communication, 9-bit UART (including parity bit), in line with standard UART protocol. When the SPIEN pin

of CSE7761 chip is connected to low level, the internal serial communication port is transferred to UART mode, at this time SDO/TX is converted to

The transmit output is TX, SDI/RX is converted to receive input RX, SCLK and SCSN control the baud rate of the UART, as shown in the following table.

Table 5-2 CSE7761 SPI command list

SPIN SCLK SCSN			describe
1	x	x	UART is in reset
0	1	1	The baud rate of UART is 38400
0	0	1	The baud rate of UART is 19200
0	1	0	The baud rate of UART is 9600
0	0	0	The baud rate of UART is 4800

Note: If an abnormality occurs in UART, you can reset UART by pulling SPIEN high and then low, and then send in the frame format of CSE7761 FF twice (sent in odd parity mode).

The UART communication format of CSE7761 is as follows:

Figure 5-3 UART communication format

The command register of UART is the same as SPI, which is also an 8-bit wide register. For read and write operations, bit 7 of the command register is used To determine whether the data transfer operation is a read operation or a write operation. For special command operations, bits 7-0 of the command register are fixed to 0xEA.

UART data transmission of CSE7761: read operation is sent by the slave end, and write operation is sent by the host end. The registers are multi-byte registers, and the most significant byte is transferred first.

The UART data verification method of CSE7761 is: the read operation is sent by the slave end, and the write operation is sent by the host end. The method is as follows:

Verify data Cdata[7:0] = ~(0xA5+CMD[7:0] + DATAn[7:0] + …… +DATA1[7:0]), that is, CMD and data Add, discard the carry, and invert the final result bit by bit;

Table 5-3 CSE7761 UART command list

Command Name	Command Register Data		describe
Read Command	{0,REG_ADR[6:0]} RDATA		Read data from the register at address REG_ADR[6:0]. Note: Reading an invalid address will return a value of 00h
Write Command	{1,REG_ADR[6:0]}	WDAT A	Write data to the register at address REG_ADR[6:0]
Write enable command 0xEA Write protect		0xE5 Enable write operation	
command 0xEA		0xDC Disable write operation	
Current channel A selects 0xEA		0x5A	Current channel A setting command, specify the current used to calculate active power The current channel of energy/reactive energy/reactive power/apparent power is open Path A
Current channel B selects 0xEA		0xA5	Current channel B setting command, specifies the current used to calculate active power The current channel of energy/reactive energy/reactive power/apparent power is open Channel
Reset Instructions	0xEA	B 0x96 Reset command. After receiving the command, the chip is reset.	

5.2.2UART frame format timing

The UART communication of CSE7761 has a fixed 11-bit method for transmitting data: 1 start bit, 8 data bits (low bit first), 1

Even parity bit (9th data bit), 1 stop bit.

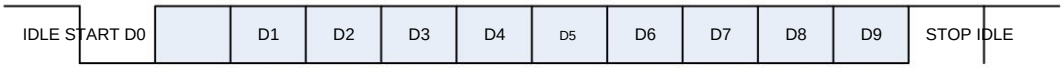


Figure 5-4 UART interface frame format

5.2.3UART Write Operation

The write operation is initiated by the host. The host sends a command byte. If it is a write command, the slave continues to receive the subsequent commands sent by the host.

Data bytes and checksum bytes.

Figure 5-5 UART write operation timing

Note:

1. The byte transmitter calculates and sends the check bit, and the byte receiver determines whether the byte transmission is valid based on the check bit;

2. If a byte is wrong, the following byte is considered to be the start of a new frame;

3. For multi-byte registers, the high byte content is transmitted first, and then the low byte content;

4. The time between bytes sent by the host is controlled by the host and has no limit;

5. The time between complete command communications is controlled by the host and is not limited;

6. For registers with write protection function, the write enable command must be written before the write operation;

7. The host calculates and sends the checksum, and the slave determines whether the frame transmission is successful based on the checksum;

For example, if the data 1234H is written to the HFConst with address 02H, the UART data is sent as follows: (each frame is sent according to the standard format frame)

1. The first frame sends 8 bits of data: 0xA5;

2. The second frame sends 8 bits of data: 0x82;

3. The third frame sends 8 bits of data: 0x12;

4. The fourth frame sends 8 bits of data: 0x34;

5. The fifth frame sends 8-bit data: 0x92; 0x92=~[0xA5+0x82+0x12+0x34];

5.2.4UART Read Operation

The read operation is initiated by the host. The host first sends the read command byte, and CSE7761 then sends the read data byte, read checksum, and

Bytes. As shown in the following figure:

Figure 5-6 UART read operation timing

Note:

1. The byte transmitter calculates and sends the check bit, and the byte receiver determines whether the byte transmission is valid based on the check bit.

If the frame is checked for errors, the byte receiving end considers the current frame to be erroneous and ends the process;

2. For multi-byte registers, the high byte content is transmitted first, and then the low byte content; 3. The time between the host sending bytes is controlled by the host side and has no restrictions; 4. The time for switching between read command and data Dataout is controlled by CSE7761: T/2 (T is the transmission time of each bit); 5. The time between CSE7761 sending data bytes is controlled by CSE7761: T (T is the transmission time of each bit);

6. The time between complete command communications is controlled by the host and has no limit; 7. The host calculates and sends the checksum, and determines whether the CSE7761 frame transmission is successful based on the checksum;

For example, to read the HFConst data with address 02H, the transmission is as follows: (each frame is transmitted according to the standard format frame) 1. The first frame sends 8 bits of data: 0xA5;

2. The second frame sends 8 bits of data: 0x02; 3. The third frame receives 8 bits of data (the upper 8 bits of HFCONST); determine whether the received check bit is correct 4. The fourth frame receives 8 bits of data (the lower 8 bits of HFCONST); determine whether the received check bit is correct

5. The fifth frame receives the verification data; determines whether the received verification data is correct.

6. Chip Features

6.1 Recommended operating conditions

Table 6-1 Recommended working conditions

parameter	symbol	Min	Typ	Max	Unit
power supply	VDD	4.5	5.0	5.5	In
	VDD	3.0	3.3	3.6	In
Reference voltage	VREF	1.23	1.25	1.27	In
Power consumption	B channel is not open (@VDD=3.3V)	·	3.7	·	m.a.
	B channel is not turned on (@VDD=5V)	·	4.3	·	m.a.
	B channel is open (@VDD=3.3V)	·	4.7	·	m.a.
	B channel is open (@VDD=5V)	·	5.5	·	m.a.
Temperature range	FACING	-40	·	+85	ÿ

Note: Power consumption @ VDD = 3.3V is a simulation value

6.2 Simulation characteristics

VDD = 5V ±10% or 3.3V ±10% ; GND = 0 V; VREF=1.25 V. MCLK = 3.579545 MHz.

Table 6-2 Analog characteristics

parameter	Symbol	Min	Typ	Max	Unit
Measurement accuracy					
Active energy measurement error	PEErr	-0.1	0	0.1	%
RMS measurement error within a dynamic range of 5000:1 at room temperature	RErr	-0.1	0	0.1	%
Active power/apparent power within a dynamic range of 1000:1 at room temperature	PERR	-0.1	0	0.1	%
Analog Input					
Differential Input Range	IIN	-800/PGA	·	+800/PGA	mVP-P
Equivalent Input	EII	70	·	·	Kÿ
Impedance Reset					
Power-on detection threshold	PMLO	2.8	2.9	2.95	In
Power-off detection threshold	PMHI	2.5	2.7	2.9	In
Temperature sensor					
Temperature error (after calibration)		·	±1	·	ÿ
Reference voltage					
Output voltage	VREF	1.23	1.25	1.27	In
temperature drift (Note 1)	TCVREF	·	5	15	ppm/ÿ

Note 1: The VREF temperature drift calculation formula within the temperature range is as follows:

$$TC_{VREF} = \left(\frac{VREF_{MAX} - VREF_{MIN}}{VREF_{AVG}}\right)\left(\frac{1}{T_{A\_MAX} - T_{A\_MIN}}\right)(1\times10^{6})$$

6.3 Digital Characteristics

VDD = 5V ±10% or 3.3V ±10% ; GND = 0 VÿMCLK = 3.579545 MHz.

Table 6-3 Digital characteristics

parameter	Symbol Min Typ Max Unit				
Master Clock					
Main clock frequency: built-in clock (Note 2) MCLK Main clock		3.507	3.579	3.65	MHz
frequency: external clock filter		·	3.579545	·	MHz
Phase compensation range (50Hz)		-2.56	·	+2.56	°
Input sampling rate ÿDCLK=MCLK/Kÿ		·	MCLK/4	·	Hz
Digital filter output bit rate High	OWR	·	MCLK/512	·	Hz
pass filter turn-off (-3dB) frequency input and		·	0.543	·	Hz
output					
UART interface speed		4800	·	9600	Hz
High-level input voltage (Note 4) Low-level input	HIV	0.5VDD	·	·	In
voltage High-level output	WILL	·	·	0.8	In
voltage IoH=4.2mA(VDD=5V) IoH=1.9mA(VDD=3.3V)	VOH	0.9*VDD	·	·	In
Low level output voltage IoL=-4.2mA (VDD=5V) IoL=-1.9mA(VDD=3.3V)	VOL	·	·	0.1*VDD	In
SPI clock frequency	SCLK	0.11	·	890	KHz
Data byte timing SCLK	t1	0.5	·	·	TSCLK
falling edge and SCSN rising edge Time between edges	t2	0.5	·	·	TSCLK

Notes:

1. When using an external clock, whether using a crystal or an external clock input, the OSCI frequency must be between 3MHz and 5MHz.
2. If external clock input is used, the duty cycle must meet 45%~55%.
3. When the power supply voltage is 5V and the input signal is 3.3V, each IO will generate 250uA current.

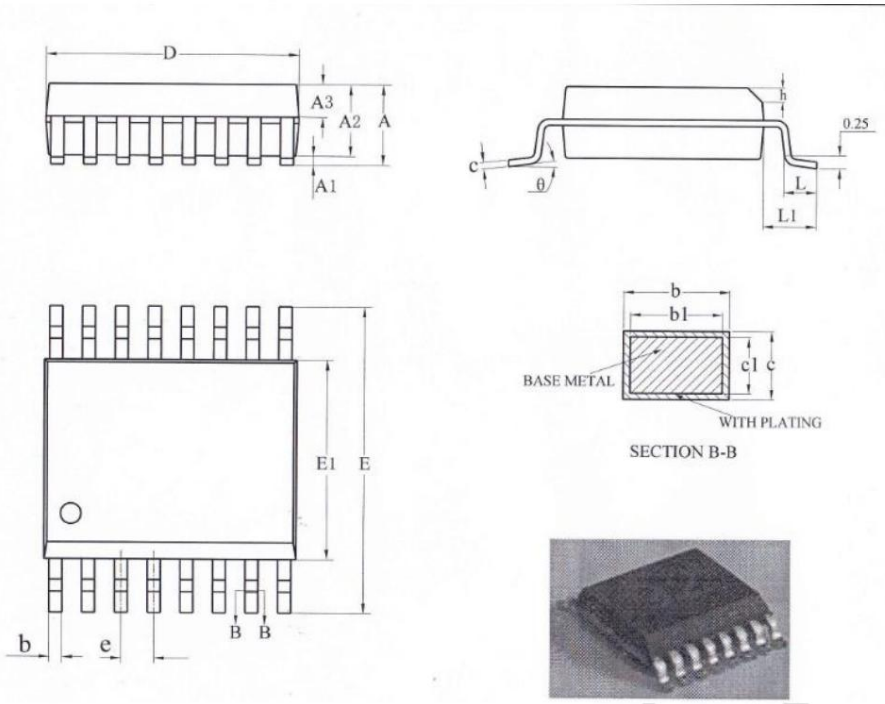
6.4 Extreme working conditions

Table 6-4 Extreme working conditions

parameter	Symbol	Min	Typ	Max	Unit
power supply	VDD	-0.3	·	+6	In
VDD to GND		-0.3	·	+6	In
V1P, V1N, V2P, V2N, V3P Analog input		-1	·	+6	In
voltage Digital input	WINES	-0.3	·	VDD+0.3 V	
voltage Digital output	FIND	-0.3	·	VDD+0.3 V	
voltage Operating	VOUTD	-0.3	·	VDD+0.3 V	
ambient temperature	FACING	-40	·	85	°C
Storage temperature	Test	-65	·	150	°C

7 -chip package

The CSE7761-SSOP16 package dimensions are as follows.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.55	0.60	0.65
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.25	—	0.50
L	0.50	0.65	0.80
L1	1.05REF		
θ	0	—	8°

Packing:

1) Chips are packed in tubes, with the first PIN of the chip facing the white plug of the tube; 2) After every twenty tubes are neatly stacked, the two ends are tied with rubber bands, and then five bundles are tied together; 3) The tubes are packed in black anti-static bags without sealing, and then put into inner boxes for packaging;

4) Every ten boxes are packed into a whole box, and the last boxes are placed on the top layer of the box. Empty boxes are used to fill the box if it is not full, and the empty boxes are placed on the bottom layer; 5) The integer packaging quantity from inside to outside is 100EA/tube, 10000EA/box, and 100000EA/box.